Ge/Si heteronanocrystal floating gate memory

Bei Li and Jianlin Liu[a)]
Quantum Structures Laboratory, Department of Electrical Engineering, University of California, Riverside, California 92521, USA

G. F. Liu and J. A. Yarmoff
Department of Physics and Astronomy, University of California, Riverside, California 92521, USA

(Received 2 July 2007; accepted 12 September 2007; published online 27 September 2007)

Metal oxide semiconductor field effect transistor memories with Ge/Si heteronanocrystals (HNCs) as floating gate were fabricated and characterized. Ge/Si HNCs with density of 5×10^{11} cm^{-2} were grown on *n*-type Si (100) substrate with thin tunnel oxide on the top. Enhanced device performances including longer retention time, faster programming speed, and higher charge storage capability are demonstrated compared with Si nanocrystal (NC) memories. The erasing speed and endurance performance of Ge/Si HNC memories are similar to that of Si NC devices. The results suggest that Ge/Si HNCs may be an alternative to make further floating gate memory scaling down possible. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2793687]

Nanocrystal floating gate memory is considered a potential candidate for the replacement of conventional continuous floating gate memory since the latter has reached tunneling limits through continuous downscaling. Many kinds of nanocrystals (NC) memory devices, such as Si,[1–3] Ge,[4,5] and metals,[6–8] have demonstrated improved performance, such as higher programming/erasing speed or longer retention times. Semiconductor NC memories, for example, Si NCs, suffer from defect level charge trapping, which is hard to control during operation. In addition, these traps are not thermally stable and cause device performance degradation after thermal annealing. Metal NC memories are also good candidates due to their higher density of states, flexibility in choosing the work function, etc., but metal and oxide reactions or interdiffusion during device integration, for example, during annealing, may potentially degrade the device performance.

In this paper, we report the fabrication and characterization of memories employing Ge/Si heteronanocrystals (HNCs) as the floating gate, including writing and erasing transients, writing saturation, endurance, and data retention. The motivation of this work is to realize longer hole retention times for *p*-channel memory devices without sacrificing the programming/erasing speed, which is a very important issue for memory device scaling. The tunneling barrier profile changes from uniform to staircase when Ge/Si HNCs replace Si NCs.[9,10] The formation of an additional quantum well for holes as a result of band offset enhances the data retention characteristics compared with Si NC memories. Simulation work[9–11] has shown better retention performance for memories with Ge/Si HNCs floating gate as compared with Si only NC memories.

Standard metal oxide semiconductor field effect transistor (MOSFET) process was used to fabricate the memories. After RCA cleaning, a 5 nm tunnel oxide was grown onto a *n*-Si(100) substrate at 850 °C followed by annealing in N_2 to suppress the interface states that originate from the thermal growth. Low pressure chemical vapor deposition (LPCVD) was used to grow Si NCs with the pressure of 400 mTorr at 600 °C, and in the same chamber Ge was selectively grown at a lower temperature on top of Si NCs at the pressure of 200 mTorr. A thin Si cap layer was deposited in order to form Ge-core/Si-shell-like structures and prevent Ge from being oxidized during the control oxide growth that followed. Control oxide layer of about 25 nm was deposited in the LPCVD furnace at 400 °C. After control oxide deposition, the wafers were transferred to another LPCVD furnace and a 350 nm polysilicon was grown. The polygate and source/drain were implanted with BF_2 to obtain the heavily doped regions. Aluminum was deposited and patterned as the contact material. Memories with Ge/Si HNCs and Si only NCs were fabricated simultaneously using the same process flow. Since these Si NCs are original features for subsequent HNC growth, excellent comparisons can be obtained between HNC memories and NC memories.

The resultant NCs were characterized by atomic force microscope (AFM) for the surface morphology and by x-ray photoelectron spectroscopy (XPS) for elemental composition analysis. The memory characterizations were done with an Agilent 4155 semiconductor parameter analysis and pulse generator at room temperature.

Figures 1(a) and 1(b) show the AFM images of Si NCs and Ge/Si HNCs grown on the tunnel oxide. The density for both of Ge/Si HNCs and Si only NCs is about 5×10^{11} cm^{-2}, while the height of the Ge/Si HNCs is larger than that of Si NCs, indicating good, self-aligned Ge/Si HNCs. The exact height cannot be determined due to AFM

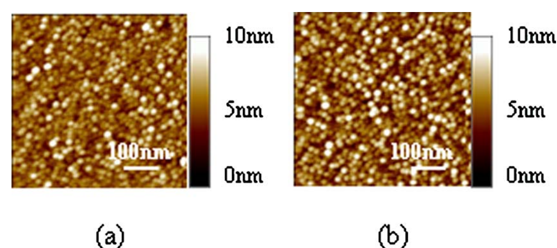

FIG. 1. (Color online) AFM images for (a) the original Si NCs and (b) the Ge/Si HNCs. The same scale is used for both images. The sharper feature in Ge/Si HNC image suggests that Ge/Si HNCs are higher due to extra growth of Ge on Si.

[a)]Author to whom correspondence should be addressed. Electronic mail: jianlin@ee.ucr.edu

 © 2007 American Institute of Physics
Downloaded 27 Sep 2007 to 138.23.166.226. Redistribution subject to AIP license or copyright, see http://apl.aip.org/apl/copyright.jsp

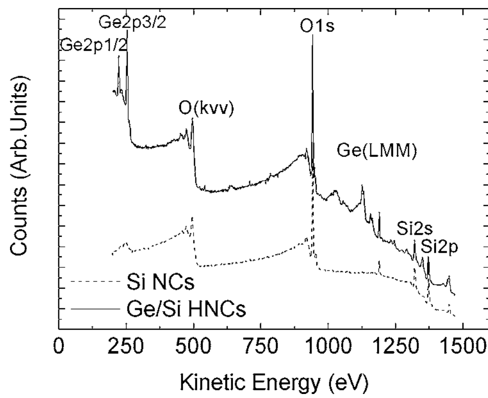

FIG. 2. XPS elemental analysis for Si NCs (bottom curve) and Ge/Si HNCs (top curve).

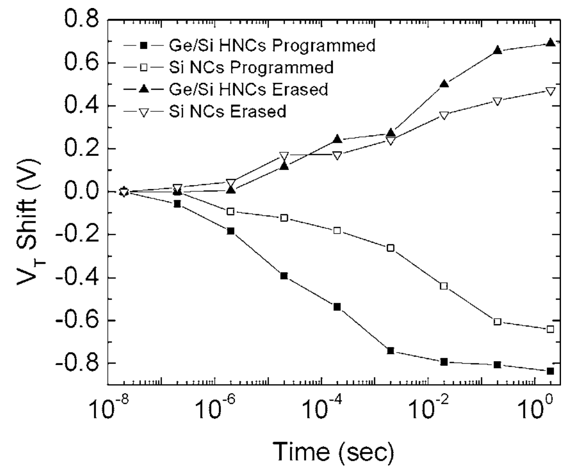

FIG. 4. Writing and erasing performance comparison between the Si NC memory devices and the Ge/Si HNC memory devices.

tip effects. The presence of Ge was verified by XPS. Figure 2 shows the XPS wide scan spectra collected for Ge/Si HNCs and Si NCs. The Ge signals are clearly observed in the Ge/Si HNC curve. To further verify the Ge/Si HNC formation, in the same LPCVD chamber, tunnel oxide without Si NCs on top was subjected to the same Ge growth conditions. In this case, no Ge signals were found in XPS, which suggests that Ge does not nucleate on the tunnel oxide at low temperature.

Figure 3 shows the transfer characteristics of Ge/Si HNC memory under the neutral, written, and erased conditions. The programming and erasing conditions are 15 V/4 s and 16 V/4 s, respectively. A memory window around 2.16 eV is clearly observed.

Figure 4 shows the programming and erasing performance comparisons between Ge/Si HNC memories and Si only NC memories. The memory window is plotted as a function of writing/erasing time. Fowler-Nordheim programming of −15 V was used to charge the device and +15 V was used to discharge it. Memories with Ge/Si HNCs as the floating gate show a faster programming speed than that of Si only NC memories. During programming holes from the inversion layer of the substrate tunnel through the oxide and get stored in the Ge NCs, so that the higher density of states for holes in Ge contributes to the faster programming speed. During erasing, both holes and electrons contribute to the tunneling current because, under the positive gate bias, holes in the Ge NCs tunnel back to the channel in the substrate and electrons from the accumulation layer also get injected into the NCs. Electron injection in the NCs dominates the erasing process due to their smaller effective mass and lower energy barrier. Therefore, a similar erasing speed for Ge/Si HNC memories was observed as compared with Si NC memories. A higher saturation level is also found for Ge/Si HNC memories, indicating that Ge/Si HNC memories have a higher charge storage capability than Si only NC memories.

Figure 5 shows the endurance characteristics of memories with Ge/Si HNCs and Si NCs. The programming and erasing conditions are gate voltages of −15 V for 20 ms and +15 V for 20 ms, respectively. After 10^5 cycles of operation, both devices show insignificant narrowing of the memory window. Memories with Ge/Si HNCs have a very similar endurance performance as the reference memories fabricated with Si NCs, indicating that the device endurance has little effect from the engineered floating gates and is mostly dependent on the control/tunnel oxide, which is the same for these devices.

Retention characteristics for Ge/Si HNC memories and Si NC memories are shown in Fig. 6. The devices were programmed with −15 V for 5 s, and the threshold voltage (V_T) shift was plotted as a function of the waiting time. It should be noted that the charge decay trends of the two devices are very similar to each other at the late stages of retention, indicating similar trap depths for the memory devices with Ge/Si HNCs and Si NCs. Nevertheless, in Si NC memory

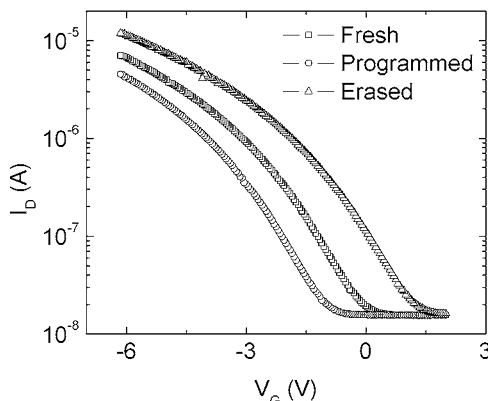

FIG. 3. Ge/Si HNC memory transfer characteristics under fresh, written, and erased conditions.

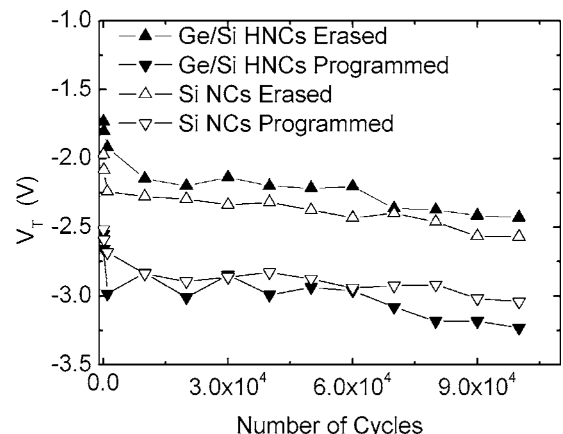

FIG. 5. Endurance characteristics of Si NC memory devices and Ge/Si HNC memory devices.

Downloaded 27 Sep 2007 to 138.23.166.226. Redistribution subject to AIP license or copyright, see http://apl.aip.org/apl/copyright.jsp

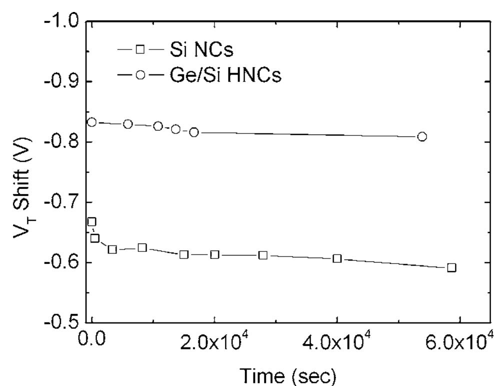

FIG. 6. Retention characteristics of Si NC memory devices and Ge/Si HNC memory devices.

significant amount of charge is stored in the shallow traps with a much larger emission rate, leading to a quick charge loss once the writing voltage is removed. These energy levels could include quantized energy levels in Si NCs due to SiO_2 barrier confinement and shallow/deep trap levels due to NC defects.[12] In Ge/Si HNC memory, due to artificially created quantum well in the Ge side, most charges from the channel during writing process are relaxed into this quantum well, leading to single, slow charge loss rate from the beginning of the retention.

In summary, Ge/Si HNC memories were fabricated and measured using standard MOSFET process. Compared with Si NC memories, Ge/Si HNC memories show a larger charge storage capacity, faster programming speed, and longer retention time. This work indicates that Ge/Si HNC memories are promising candidates for *p*-channel memory to replace conventional flash memory and Si NC memory and further improve device scaling.

The authors acknowledge the financial and program support of the Focus Center Research Program (FCRP) on Function Engineered NanoArchitectonics (FENA).

[1] S. Tiwari, F. Rana, K. Chan, L. Shi, and H. Hanafi, Appl. Phys. Lett. **69**, 1232 (1996).

[2] V. Turchanikov, A. Nazarov, V. Lysenko, E. Tsoi, A. Salonidou, and A. G. Nassiopoulou, Physica E (Amsterdam) **38**, 80 (2007).

[3] C. Y. Ng, T. P. Chen, D. Sreeduth, Q. Chen, L. Ding, and A. Du, Thin Solid Films **504**, 25 (2006).

[4] M. Kanoun, C. Busseret, A. Poncet, A. Souifi, T. Baron, and E. Gautier, Solid-State Electron. **50**, 1310 (2006).

[5] S. Duguay, A. Slaoui, J. J. Grob, M. Kanoun, S. Burignat, and A. Souifi, Mater. Sci. Eng., B **124-125**, 488 (2005).

[6] Z. T. Liu, M. Kim, V. Narayanan, and E. C. Kan, Superlattices Microstruct. **28**, 393 (2000).

[7] D. T. Zhao, Y. Zhu, and J. L. Liu, Solid-State Electron. **50**, 268 (2006).

[8] S. Kolliopoulou, P. Dimitrakis, P. Normand, H.-L. Zhang, N. Cant, S. D. Evans, S. Paul, C. Pearson, A. Molloy, M. C. Petty, and D. Tsoukalas, Microelectron. Eng. **73-74**, 725 (2004).

[9] H. G. Yang, Y. Shi, L. Pu, R. Zhang, B. Shen, P. Han, S. L. Gu, and Y. D. Zheng, Appl. Surf. Sci. **224**, 394 (2004).

[10] D. T. Zhao, Y. Zhu, R. G. Li, and J. L. Liu, IEEE Trans. Nanotechnol. **5**, 37 (2006).

[11] D. T. Zhao, Y. Zhu, R. G. Li, and J. L. Liu, Solid-State Electron. **50**, 362 (2006).

[12] Y. Shi, K. Saito, H. Ishikuro, and T. Hiramoto, J. Appl. Phys. **84**, 2358 (1998).

Downloaded 27 Sep 2007 to 138.23.166.226. Redistribution subject to AIP license or copyright, see http://apl.aip.org/apl/copyright.jsp