Fabrication and characterization of $TiSi_2/Si$ heteronanocrystal metal-oxide-semiconductor memories

Yan Zhu, Bei Li, and Jianlin Liu[a)]
Quantum Structures Laboratory, Department of Electrical Engineering, University of California, Riverside, California 92521

(Received 9 August 2006; accepted 13 January 2007; published online 19 March 2007)

$TiSi_2/Si$ heteronanocrystals on ultrathin oxide was fabricated with self-aligned silicidation method. Compared with Si nanocrystal memory device, $TiSi_2/Si$ heteronanocrystal metal-oxide-semiconductor memory device shows higher writing saturation level, faster writing/erasing speed, longer retention, and larger memory window. Therefore, heteronanocrystals are very promising to replace Si nanocrystals for future nonvolatile memory applications. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2710441]

I. INTRODUCTION

Nonvolatile memory devices with semiconductor or metal nanocrystals as storage elements in metal-oxide-semiconductor (MOS) field effect transistors have attracted much attention from researchers in both industry and academic institutions.[1–7] Besides these, dielectric nanocrystals (Al_2O_3, HfO_2, Si_4N_3, etc.)[8–10] were also reported. Intrinsically, semiconductor nanocrystals encounter the issue of defect-related trapping. The large amount of defect-induced charge traps plays a dominant role in the memory operations because of the relatively smaller density of states in the nanocrystals. Therefore, the postannealing can dramatically affect the device performance. The situation becomes even more serious for the dielectric nanocrystals since the defect-induced traps are the only storage nodes for charge retention. The higher trap levels also induce the erasing saturation as has already been known in the silicon-oxide-nitride-oxide-silicon (SONOS) memory device.[11] An alternative is metal nanocrystals with high density of states.[3–6] Nevertheless, one drawback of using metal nanocrystals is the metal/oxide reaction in device integration.

In our previous paper, we reported the research results on MOS memory devices using titanium silicide/Si ($TiSi_2/Si$) heteronanocrystals as the floating gates.[12] We investigated the memory effect of a $TiSi_2/Si$ heteronanocrystal memory with capacitance-voltage sweep method. In this work, we report our detailed study of the transient processes of programming, erasing and retention of a $TiSi_2/Si$ heteronanocrystal MOS memory. $TiSi_2/Si$ heteronanocrystals can be achieved using self-aligned silicidation technique based on Si nanocrystals. Figure 1 shows the band diagrams of $TiSi_2/Si$ heteronanocrystal memory in retention, programming, and erasing operation modes. The work function difference between $TiSi_2$ and Si creates a deep quantum well in $TiSi_2$. For charge storage, the band offset acts as a barrier in addition to tunnel oxide that prolongs the retention time significantly [Fig. 1(a)]. During writing under high voltage [Fig. 1(b)], electrons tunnel through the tunnel oxide barrier and are immediately relaxed into the silicide. This suggests that tunneling probability in writing process of $TiSi_2/Si$ heteronanocrystal memory is mainly dependent on the band offset of the tunnel oxide in the conduction band (about 3 eV), similar to the case of Si nanocrystal memory. Similar situation also applies to the erasing process [Fig. 1(c)]. As the negative gate voltage is high enough, the extra barrier becomes transparent and does not hinder the erasing efficiency. The metallic property of silicide leads to higher density of states and stronger coupling between the nanocrystals and the channel. This allows easier tunneling during erasing and writing. The metallic nature of silicide also introduces less Coulomb blockade effect. Therefore, there is less Coulomb repulsion from the subsequent charge so that the tunneling will be less depressed as the writing or erasing time increases. This also gives the increase of writing and erasing speeds as compared to a Si nanocrystal memory device. Furthermore, metallic $TiSi_2$ is more thermally stable than metal Ti. The Si dot at the bottom also helps to prevent the diffusion of metal atoms into the oxide during thermal treatment and favors the device reliability. Therefore, $TiSi_2/Si$ heteronanocrystal floating gate memory devices are expected to have superior performances.

II. FABRICATION AND MEASUREMENT

Thermal oxide with thickness of about 5 nm was grown on a chemically cleaned 4″ p-type Si at 850 °C. It was annealed in nitrogen at 900 °C for 30 s before the nanocrystal deposition to release the stress and densify the oxide layer. This step was found to be very critical to depress metal/oxide reaction for better charge retention. Si nanocrystals were grown at 600 °C for 10 s with the SiH_4 pressure of 136 mtorr in a low pressure chemical vapor deposition (LPCVD) system. The $TiSi_2/Si$ heteronanocrystals were fabricated with a two-step silicidation method. First a 2-nm-thick (nominal) blanket metal Ti was deposited onto the sample. The first annealing was performed subsequently in nitrogen at 750 °C for 20 s. The unreacted Ti metal on top of nanocrystals as well as in between nanocrystals was removed in selective etchant ($NH_4OH:H_2O_2:H_2O=1:1:5$). Discrete $TiSi_2/Si$ heteronanocrystals with the same dot den-

a)Author to whom correspondence should be addressed; electronic mail: jianlin@ee.ucr.edu

0021-8979/2007/101(6)/063702/4/$23.00 © 2007 American Institute of Physics

Downloaded 19 Mar 2007 to 138.23.166.226. Redistribution subject to AIP license or copyright, see http://jap.aip.org/jap/copyright.jsp

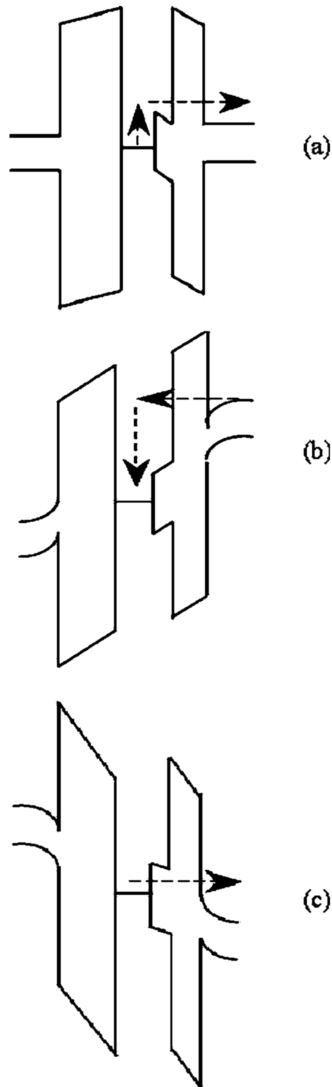

FIG. 1. Band diagram of the silicide/silicon heteronanocrystal memory in the conditions of (a) retention, (b) programming, and (c) erasing.

sity as original Si nanocrystals were formed in this stage. The second annealing was performed at 880 °C for 30 s after the metal removal to form more thermally robust $TiSi_2$ dots on Si dots. The sample was then capped with control oxide with thickness of about 17 nm in a low-temperature oxide CVD furnace. Finally, aluminum pads $(200 \times 200\ \mu m^2)$ were deposited on the front and back sides of the sample to form the MOS capacitor memory. The resultant nanocrystals were characterized by atomic force microscope (AFM) for the surface morphology and by secondary ion mass spectroscope (SIMS) for the element composition analysis. The memory characterizations were done with Agilent *LCR* meter and pulse generator at room temperature. The memory window and time-dependent transient capacitance (*C*-*t*) were measured with the *C*-*V* sweep and the constant capacitance method.[12]

III. RESULT AND DISCUSSION

Figure 2(a) shows an AFM image of the as-grown Si nanocrystals. The dot diameter is about 13 nm and the dot density is around $5 \times 10^{11}\ cm^{-2}$. Figure 2(b) shows an AFM

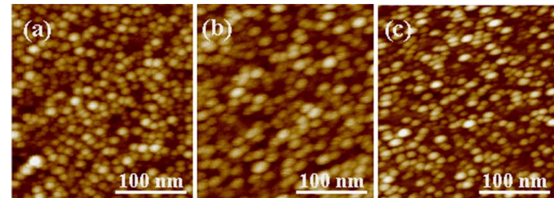

FIG. 2. (Color online) AFM images for (a) the original Si dots, (b) the $TiSi_2/Si$ heteronanocrystals, and (c) the $TiSi_2/Si$ heteronanocrystals after HF etching.

image of the $TiSi_2/Si$ heteronanocrystals. It is found that the dot density does not change as compared to the original Si nanocrystals, suggesting very good self-aligned silicidation process. This density is almost one order of magnitude higher than that of the previous heteronanocrystals.[12] Figure 2(c) shows an AFM image of the $TiSi_2/Si$ heteronanocrystal sample after diluted HF etching. Since diluted HF etches silicide rather than Si, the smaller dots in the image are the remaining Si nanocrystals. Figure 3 shows the SIMS elemental depth profile of the MOS device containing $TiSi_2/Si$ heteronanocrystals. A singularity distribution of Ti signal in the oxide can be found, again indicating the formation of silicide dots on top of Si nanocrystals and negligible Ti diffusion after silicidation. The thickness of $TiSi_2$ part on Si nanocrystal is estimated to be about 3 nm from nanocrystal height difference between the Si nanocrystals and the $TiSi_2/Si$ heteronanocrystals in AFM studies.

Figure 4 shows a typical *C*-*V* sweep result for the MOS memory devices with $TiSi_2/Si$ heteronanocrystals and Si nanocrystals. The sweep began from inversion region to accumulation region and back to inversion region again. The voltage sweep rate is 0.6 V/s. *C*-*V* curves exhibit evident hysteresis with a voltage shift of around 2.8 and 1.5 V between the forward and reverse sweep branches for the $TiSi_2/Si$ hetero-nanocrystal and Si nanocrystal MOS devices, respectively. In other words, strong memory effects are observed. The $TiSi_2/Si$ heteronanocrystal memory shows a larger charge storage capacity than that of the Si nanocrystal memory.

Figure 5 shows the programming transient processes under a writing voltage of 20 V for MOS devices with $TiSi_2/Si$ heteronanocrystals and Si nanocrystals. The writing was per-

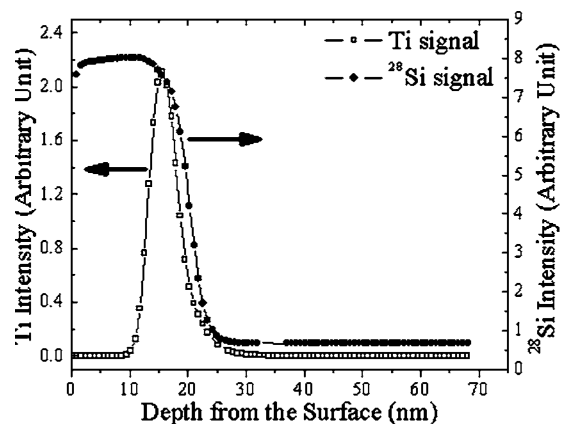

FIG. 3. SIMS depth profile for the $TiSi_2/Si$ heteronanocrystal MOS device.

Downloaded 19 Mar 2007 to 138.23.166.226. Redistribution subject to AIP license or copyright, see http://jap.aip.org/jap/copyright.jsp

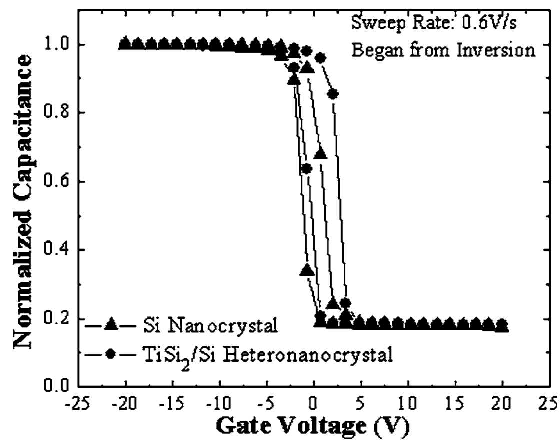

FIG. 4. *C-V* sweep measurement for the $TiSi_2/Si$ heteronanocrystal MOS memory and Si nanocrystal MOS memory.

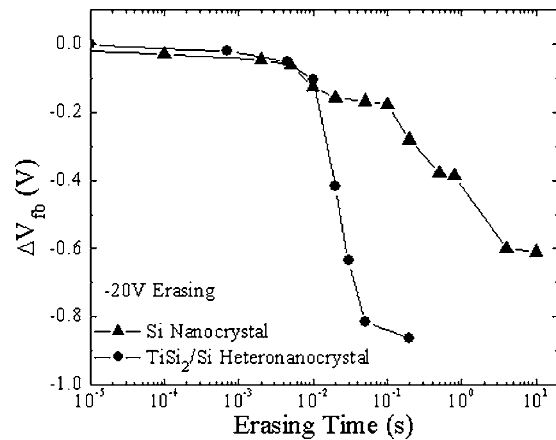

FIG. 6. Erasing performance comparison between the Si nanocrystal memory device and the $TiSi_2/Si$ heteronanocrystal memory device.

formed with light illumination to prevent the devices from reaching deep depletion region during writing. The flatband shift (ΔV_{fb}) saturates as the time increases. This saturation can be explained by the Coulomb blockade effect caused by the small dot size. However, the programming of the $TiSi_2/Si$ heteronanocrystal device slows as ΔV_{fb} reaches 1.4 V, which is much higher than that of the Si nanocrystal memory device (0.8 V). This indicates a larger charge storage capacity for the $TiSi_2/Si$ heteronanocrystal memory than the Si nanocrystal memory. Due to metallic nature, $TiSi_2$ dots have larger density of states than pure-Si nanocrystals, therefore $TiSi_2/Si$ heteronanocrystals can accommodate much more charge. In addition, due to less significant Coulomb blockade effect and stronger coupling between the $TiSi_2/Si$ heteronanocrystal floating gate and the substrate, the programming speed is faster for heteronanocrystal device. For example, a ΔV_{fb} of 0.85 V can be reached with a writing time of about 3 ms at 20 V. As a comparison, it takes 0.7 s for the Si nanocrystal memory device to achieve the same ΔV_{fb}.

Figure 6 shows the erasing performance comparison between the Si nanocrystal device and the $TiSi_2/Si$ heteronanocrystal device. The erasing saturation is observed for both Si nanocrystal device and $TiSi_2/Si$ heteronanocrystal device. However, the $TiSi_2/Si$ heteronanocrystal device exhibits a much faster erasing speed and a larger saturation level with the same erasing voltage of −20 V. With an erasing time of 50 ms, the $TiSi_2/Si$ heteronanocrystal memory exhibits an erasure level of −0.85 V, and then the erasing slows down. The erasing of a Si dot device saturates at $\Delta V\text{th}=-0.61$ V when erasing time approaches 10 s.

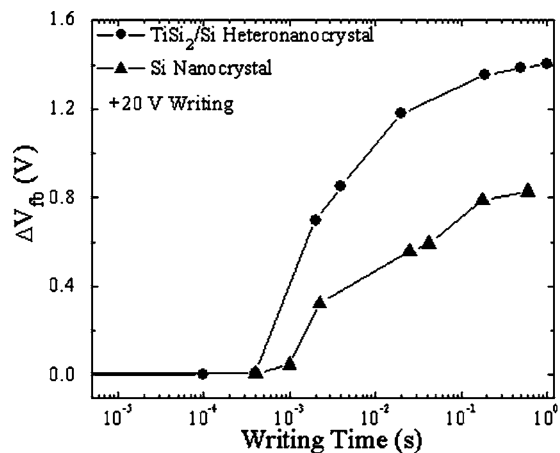

FIG. 5. Writing performance comparison between the Si nanocrystal memory device and the $TiSi_2/Si$ heteronanocrystal memory device.

The differences of the erasing speed and saturation level between the two devices can be explained by the similar mechanism for the writing case. Because the barrier for hole tunneling (about 5 eV) is higher than the barrier for electron tunneling, erasing is dominated by the process of electron removal from the floating gate. The electron removal from the neutral nanocrystals leads to the positively charged nanocrystals. The more electrons are removed, the more positive potential the nanocrystal has. The increased positive potential in consequence inhibits further removal of electrons. As a matter of fact, this saturation process is a hole Coulomb blockade process. Again due to the metallic property of silicide, $TiSi_2/Si$ heteronanocrystal memory shows less saturation than that for Si nanocrystal memory device. It is also found that the erasing speed is slower than the writing speed at the same absolute operation voltage for either $TiSi_2/Si$ heteronanocrystal memory or Si nanocrystal memory. This is due to the fact that the electrons need to overcome a higher barrier than that in writing case as they are confined in the $TiSi_2$ quantum well of heteronanocrystal or trapped in defect levels of Si nanocrystal.

The charge retention characteristics of the two devices were compared and shown in Figure 7. The writing was carried out with a writing voltage of 20 V for 1 s, which led to a saturated ΔV_{fb} of 1.41 and 0.82 V for $TiSi_2/Si$ heteronanocrystal MOS and Si nanocrystal MOS devices, respectively. $TiSi_2/Si$ heteronanocrystal device possesses a much slower charge loss rate, which is owed to the deep quantum well formed by the $TiSi_2/Si$ band offset. It is expected that even after ten years of retention, the remaining charge still holds 91% of the initial written value. However, there is only 63% of the initial charge remaining after ten years for the Si nanocrystal memory device. It should be noted that the charge decay trends of the two devices are very similar to each other at the late stage of retention, indicating the similar

Downloaded 19 Mar 2007 to 138.23.166.226. Redistribution subject to AIP license or copyright, see http://jap.aip.org/jap/copyright.jsp

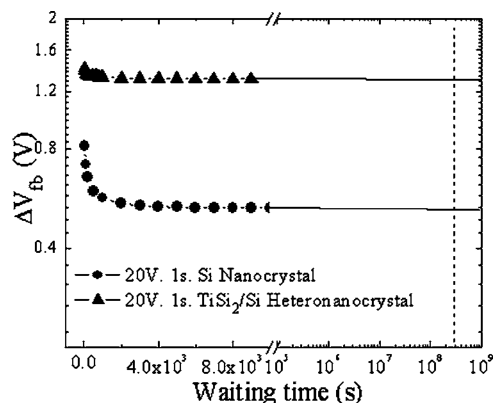

FIG. 7. Retention characteristics of the MOS devices with Si nanocrystals and $TiSi_2/Si$ heteronanocrystals. The charge amount is plotted in logarithmic scale while time in linear scale.

trap depths for the memory devices with $TiSi_2/Si$ and Si nanocrystals. Nevertheless, in Si nanocrystal memory most of the charges are stored in the shallow traps, leading to a quick charge loss once the writing voltage is removed. Assuming a constant back-tunneling probability, the charge decay from an energy level follows a simple exponential law.[13] In other words, charge amount, or ΔV_{fb}, in logarithmic scale depends linearly on time. As can be seen in Fig. 7, the ΔV_{fb} decay of the $TiSi_2/Si$ nanocrystal memory follows almost a single linear trend. This suggests that most of the initially written charges are localized in the silicide portion (quantum well) of the heteronanocrystals. The Si nanocrystal memory shows a significant charge loss in the first 2000 s, followed by a slow decay with the decay constant (the slope) similar to that of the $TiSi_2/Si$ heteronanocrystal memory. This indicates that multiple energy levels are involved in charge storage when Si nanocrystals are used solely as floating gate. These energy levels could include quantized energy levels in Si nanocrystals due to SiO_2 barrier confinement and shallow/deep trap levels due to nanocrystal defects.[14]

IV. SUMMARY

$TiSi_2/Si$ heteronanocrystals were fabricated using the silicide technique based on Si nanocrystals on silicon dioxide films. The MOS capacitor containing these heteronanocrystals exhibits much better charge retention characteristics, wider memory window, and less writing/erasing saturation, as compared to the Si nanocrystal memory device. Therefore $TiSi_2/Si$ heteronanocrystal is a promising candidate to replace Si nanocrystal for the next-generation floating gate flash memory devices.

ACKNOWLEDGMENTS

The authors acknowledge the financial and program support of the Microelectronics Advanced Research Corporation (MARCO) and its Focus Center on Function Engineered NanoArchitectonics (FENA) and the National Science Foundation (ECS-0622647).

[1] S. Tiwari, F. Rana, K. Chan, L. Shi, and H. Hanafi, Appl. Phys. Lett. **69**, 1232 (1996).
[2] Q. Wan, C. L. Lin, W. L. Liu, and T. H. Wang, Appl. Phys. Lett. **82**, 4708 (2003).
[3] Z. T. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, IEEE Trans. Electron Devices **49**, 1606 (2002).
[4] C. H. Lee, J. Meteer, V. Narayanan, and E. C. Kan, J. Electron. Mater. **34**, 1 (2005).
[5] J. J. Lee and D. L. Kwong, IEEE Trans. Electron Devices **52**, 507 (2005).
[6] T. C. Chang, P. T. Liu, S. T. Yan, and S. M. Sze, Electrochem. Solid-State Lett. **8**, G71 (2005).
[7] S. Choi, S. S. Kim, M. Chang, H. S. Hwang, S. H. Jeon, and C. W. Kim, Appl. Phys. Lett. **86**, 123110 (2005).
[8] J. H. Chen, W. J. Yoo, D. S. H. Chan, and L. J. Tang, Appl. Phys. Lett. **86**, 073114 (2005).
[9] Y. H. Lin, C. H. Chien, C. T. Lin, C. Y. Chang, and T. F. Lei, IEEE Electron Device Lett. **26**, 154 (2005).
[10] S. Y. Huang, K. Arai, K. Usami, and S. Oda, IEEE Trans. Nanotechnol. **3**, 210 (2004).
[11] M. Sadd, J. A. Yater, J. Bu, C. M. Hong, W. M. Paulson, C. T. Swift, R. Singh, L. Parker, and M. G. Khazhinsky, Proceedings of the IEEE Non-Volatile Semiconductor Memory Workshop, 2003 (unpublished), p. 71.
[12] Y. Zhu, D. T. Zhao, R. G. Li, and J. L. Liu, Appl. Phys. Lett. **88**, 103507 (2006).
[13] M. She and T.-J. King, IEEE Trans. Electron Devices **50**, 1934 (2003).
[14] Y. Shi, K. Saito, H. Ishikuro, and T. Hiramoto, J. Appl. Phys. **84**, 2358 (1998).

Downloaded 19 Mar 2007 to 138.23.166.226. Redistribution subject to AIP license or copyright, see http://jap.aip.org/jap/copyright.jsp