Numerical investigation of transient capacitances of Ge/Si heteronanocrystal memories in retention mode

Yan Zhu, Dengtao Zhao, and Jianlin Liu[a)]
Quantum Structures Laboratory, Department of Electrical Engineering, University of California, Riverside, California 92521

(Received 22 February 2006; accepted 6 December 2006; published online 13 February 2007)

Transient capacitances were numerically investigated for Ge/Si heteronanocrystal memories. Flatband voltage shifts (ΔV_{fb}) were obtained. The results suggest that the Ge/Si heteronanocrystal memories have significantly longer data retention compared with the memories embedding Si nanocrystals only. It is also found that larger heteronanocrystal leads to longer retention, larger device capacitance, and smaller ΔV_{fb}. © *2007 American Institute of Physics*.
[DOI: 10.1063/1.2434947]

I. INTRODUCTION

Nanocrystal memory is a promising candidate to replace extended floating gate flash memory on the route of aggressive scaling of semiconductor nonvolatile memory cell to achieve high device density, and low voltage operation or low power consumption.[1–5] In order to further optimize nanocrystal-based device performance, it is important to study its dynamic characteristics.[6] The reported experimental techniques to obtain dynamic processes in nanocrystal memories include transient current technique,[7,8] transient threshold voltage method,[8,9] and transient capacitance method.[10–13] Among these techniques, transient capacitance method is a convenient method as it only requires a metal-oxide-semiconductor (MOS) structure, in comparison with transient source-to-drain current method, where source, drain, and gate have to be defined. For example, Wahl *et al.*[10] have experimentally investigated the charging and discharging of Si nanocrystal memories by measuring capacitances as a function of time at certain gate voltages. It is found that device capacitances strongly depend on charging and discharging status of the embedded nanocrystals. In addition, the discharging branch of *C-V* indicates a combination of two mechanisms with different discharging constants.[10]

Compared with a great deal of experimental efforts, a detailed theoretical insight on the charging/discharging properties of nanocrystal memories is still lacking. Moreover, as the device continues scaling down to demand thinner tunneling oxide, the consideration of the dynamic tunneling leakage current becomes crucial. In order to reduce the tunneling leakage current to maintain long retention characteristics of memory devices where the tunneling oxide gets thinner, Ge/Si heteronanocrystals were proposed to replace Si nanocrystals[14–16] as floating gate in the memory design. The Ge/Si heteronanocrystal system provides an additional quantum well for a hole to store in the Ge side as a result of the valence band offset at the Ge/Si interface. This additional well prolongs the retention time significantly while changes the writing/erasing speed insignificantly.[14–16] Experimentally, such Ge/Si heteronanocrystals are achievable. First, high-density Si nanocrystals can be formed on tunneling oxide in a chemical vapor deposition (CVD) furnace. Then the substrate temperature is decreased to be on or below 400 °C and GeH_4 or Ge_2H_6 can be introduced into the same CVD to achieve selective epitaxial growth (SEG) of Ge onto Si dots only. At such growth condition, Ge dots can only be formed on crystalline Si dots rather than on amorphous tunneling SiO_2. As a matter of fact, similar process has been used to produce coshell Ge/Si nanowires.[17]

In this paper, we investigate numerically the transient capacitances of nanocrystal memories including Si nanocrystal memory and Ge/Si heteronanocrystal memory. A simple physical model to consider both the quantum confinement effect and Coulomb blockade effect is used for capacitance calculations in the dynamic discharging process. The transient flatband voltage shifts (ΔV_{fb}) are obtained with a constant-capacitance method,[3] which directly reflects retention characteristics of these memories.

II. MODEL AND THEORY

The structure of a Ge/Si heteronanocrystal memory is schematically shown in Fig. 1(a). For all calculations, the total thickness of the control oxide, the height of Ge dot, and the height of Si dot are fixed at 10 nm to ensure that the comparison is reasonable. The corresponding valence band structure in flatband condition is plotted in Fig. 1(b). Only the valence band offset is considered for the *p*-channel memory. To the first order of accuracy, no strain in the heteronanocrystal system is involved. Under this circumstance, a valence band offset of 0.47 eV was assumed.[18] The conduction band offset (ΔE_C) of Ge/Si is very small and is not shown. Both Si and Ge components are assumed to be cubic shape. The dot density is fixed at 6×10^{11} cm^{-2}.

During retention, two currents are considered. One is the electron current leaking from the substrate to the nanocrystals. The other one is the hole current from the nanocrystal back to the substrate. In the simulation, the interface carrier density and interface field are derived from two-dimensional Poisson-Boltzmann's equation. To simplify the problem, each nanocrystal is modeled as an infinitely long wire. Periodic boundary condition is used in the lateral direction. In the vertical direction, Ohmic Al/Si contacts are assumed. Since *n*-type substrate has a similar work function to alumi-

[a)]Electronic mail: jianlin@ee.ucr.edu

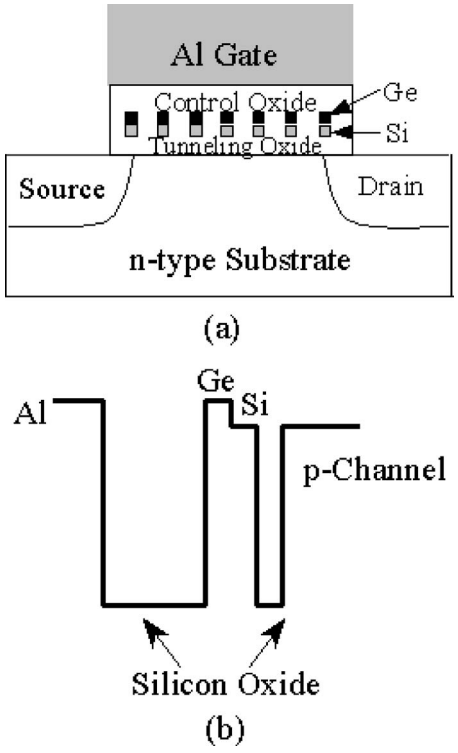

FIG. 1. (a) Device structure of a Ge/Si heteronanocrystal floating gate memory and (b) the corresponding band diagram in the direction normal to the substrate plane.

num, the flatband voltage is set to be zero. The aluminum gate and substrate are biased to V_g and zero, respectively. These two voltage values are set to be the boundary conditions in vertical direction.

Based on the surface field, the confinement status of the electrons or holes is obtained and used for tunneling current calculation.[19] Briefly, the tunneling leakage current density from the substrate to the floating dots can be expressed as

$$J_{\text{sub-dot},E} = q\int_{E_{\text{shift}}\leqslant E} T(E)f(E)\rho(E)F_{1/2}(E)dE, \tag{1}$$

where $f(E)$ is the impact frequency, $\rho(E)$ the density of states, $F_{1/2}(E)$ the Fermi-Dirac distribution function, and $T(E)$ the tunneling probability. E_{shift} is the Si valence or conduction band shift due to the nanocrystal's quantum confinement effect. The impact frequency reads[19]

$$f(E) = 0.6\frac{2q}{(3\pi\hbar m_{\text{Si},\perp})^{1/3}}\left(\frac{\varepsilon_{\text{ox}}F_{\text{ox}}}{\varepsilon_{\text{Si}}}\right)^{2/3}, \tag{2}$$

where $\hbar$, $m_{\text{Si},\perp}$, ε_{ox}, F_{ox}, and ε_{Si} are reduced Planck's constant, hole (or electron) effective mass perpendicular to the substrate, dielectric constant of SiO_2, electric field in SiO_2 layer, and Si dielectric constant, respectively. The density of states of the two-dimensional (2D) confined hole or electron gas is[19]

$$\rho(E) = \frac{m_{\text{Si},\|}}{\pi\hbar^2}, \tag{3}$$

where $m_{\text{Si},\|}$ is the hole or electron effective mass in the confined plane of accumulation or inversion layer of the substrate. The field in oxide layer F_{ox} can be obtained by solving the Poisson equation. The tunneling probability $T(E)$ is obtained using the transfer matrix method.[20,21] Briefly, an arbitrary barrier can be approximated with N slices. In each slice, the potential keeps constant. The approximation can be sufficiently precise if N is large enough. The wave function with each potential sheet can be expressed as the sum of a forward and a backward wave. The relation between the wave amplitudes in sheet i and $i+1$ can be obtained by using the boundary conditions for energy and momentum conservation, which finally leads to[21]

$$\begin{pmatrix} A_{N+1} \\ B_{N+1} \end{pmatrix} = T\begin{pmatrix} A_0 \\ B_0 \end{pmatrix} = \begin{pmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{pmatrix}\begin{pmatrix} A_0 \\ B_0 \end{pmatrix}, \tag{4}$$

where T is the transfer matrix and A_i and B_i $(i=1-N+1)$ are the amplitudes of the forward and backwards wave components in the ith slice of the barrier. Since $A_1=1$ and $B_n=0$ means a unit forward wave in the incident medium, there is no backward component at the exit side; one then obtains the tunneling coefficient $D(E_x)$,[20,21]

$$D(E_x) = \frac{k_{N+1}(E_x)m_0^*}{k_0(E_x)m_{N+1}^*}|A_{N+1}(E_x)|^2, \tag{5}$$

where the wave vector k_i in the ith slice verifies

$$k_i = \frac{\sqrt{2m_i^*(E-V_i)}}{\hbar}, \tag{6}$$

and V_i is the potential in the ith potential sheet. The potential distribution is obtained by solving Poisson equation with finite-difference method by considering the contribution of the charge if it is already injected into the nanocrystal.

During retention process, besides the electron current from the substrate to the nanocrystals [Eq. (1)], the hole current from the nanocrystals to the substrate should be considered as well, which is written as

$$I_{\text{dot-sub}} = Q_{\text{dot}}\sum_{i=n}^{\infty}\exp\left[\frac{-(E_i-E_1)}{k_BT}\right]f(E_i)T(E_i), \tag{7}$$

where E_i, E_0, and K_B are the ith excited and ground states of the heteronanocrystal and Boltzmann's constant, respectively. Q_{dot} is the charge quantity in the nanocrystal. The integer number n is the quantum number, from which the wave function of the hole covers both Ge and Si regions of the heteronanocrystal. The term $\exp[-(E_i-E_1)/k_BT]$ in Eq. (7) represents the detrapping coefficient since a hole confined in the Ge region of the Ge/Si heteronanocrystal should be first thermally activated to the nth excited state, where nth state is the first state whose energy level is higher than the valence band edge of Si dot. This means that the wave function of nth state spreads to cover both Ge and Si regions. Only those excited electrons which have energy higher than nth state can tunnel back to the substrate. This process is very similar to the detrapping process described in the paper of She and King.[6] The eigenenergies and corresponding wave functions are calculated using an improved shooting method[22] with the effective mass approximation model. In the channel plane, the Ge/Si heteronanocrystal is treated as standard quantum box. In the vertical direction, finite quan-

tum confinement as a result of finite band offset is used. The shooting method is used without considering the band structure nonparabolicity. Based on the eigenenergies, Weinberg's impact frequency $f(E_i)$ can be written as[23]

$$f(E_i) = \frac{E_i - E_1}{h}, \tag{8}$$

where h is Planck's constant. Then the total tunneling current is expressed as

$$I_{\text{total}} = J_{\text{sub-dot}} A_{\text{dot}} + I_{\text{dot-sub}}, \tag{9}$$

where $J_{\text{sub-dot}}$ is the electron current density, $J_{\text{dot-sub}}$ is the hole current density, and A_{dot} is the interfacial area between the nanocrystal and the tunnel oxide. Due to strong Coulomb blockade effect from small nanocrystals considered in our simulation, only single charge storage at the beginning of the retention is investigated.

The tunneling current is refreshed every time step Δt and the charge amount inside the nanocrystal as a function of time is then obtained. Based on this charge quantity, the variation of the carrier sheet density ($\Delta\sigma$) near the oxide/substrate interface is obtained by solving Poisson-Boltzmann equation with the given gate bias V_g and $V_g + \Delta V$, respectively. The capacitance per unit area is then defined as

$$C = \frac{s\sum_{i=1}^{n}\sum_{j=1}^{m}\Delta\sigma_{ij}}{\Delta V}, \tag{10}$$

where s is the area of the finite-difference grid in solving Poisson equation, in which the channel is divided into $m \times n$ grids. The simulated device has a channel area of $0.16 \times 0.16\ \mu\text{m}^2$, corresponding to the physical device dimensions of a memory at 90 nm technology node.

III. RESULT AND DISCUSSION

The time-evolution behaviors are compared for the memories with Ge/Si hetero-nanocrystals and Si nanocrystals, respectively, as shown in Fig. 2(a) for the charge value (Q_{dot}) and (b) for the capacitance (C), respectively, at zero bias. The tunneling oxide thicknesses (T_{ox}) are 2.0 nm. It is obvious that compared to Si nanocrystals, Ge/Si heteronanocrystals dramatically improve the retention. The time to lose one hole can be as long as ~3 yr (10^8 s) for the Ge/Si heteronanocrystal (2/2 nm) memory while it is only 17 min (~10^3 s) for the Si nanocrystal memory. If we define the retention time as the time when 20% charge in floating gate is lost,[6] $\tau \sim 2.7 \times 10^5$ s can be achieved for the Ge/Si heteronanocrystal (2/2 nm) device while it is only 30 s for the Si nanocrystal (4 nm) memory. The corresponding capacitance decay curves for Ge/Si and Si nanocrystal memories are plotted in Fig. 2(b) against time. Holes stored in the nanocrystal floating gate set the n-type substrate to the accumulation region to some extent, which corresponds to a larger capacitance than that near the flatband condition (neutral device). As the holes leak away, or are recombined by electrons from the substrate, the oxide/substrate interface changes gradually from accumulation to flatband condition, which results in gradually decreased capacitance. It is noticed in Fig. 2(b) that the Ge/Si heteronanocrystal memory has slower capacitance decay than that of the Si nanocrystal memory, indicating better retention.

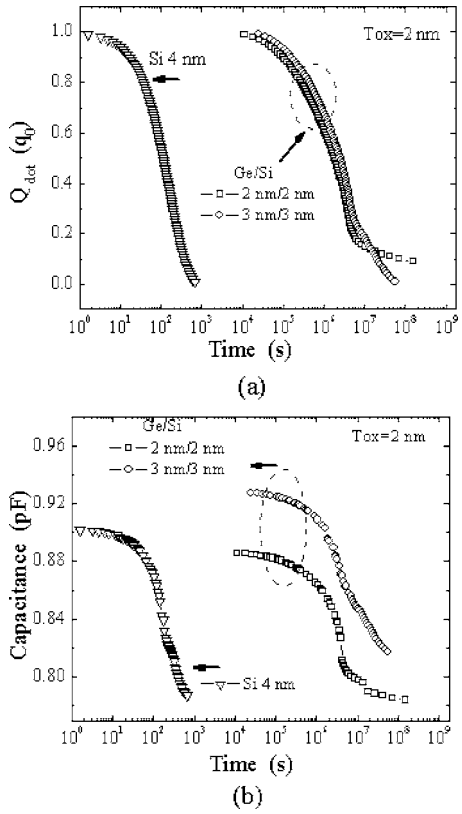

FIG. 2. (a) The charge loss transient and (b) the capacitance decay of a Si nanocrystal memory and Si/Ge heteronanocrystal memories.

The size of the heteronanocrystal plays an important role for charge storage.[15] The device with smaller nanocrystals (Ge/Si=2/2 nm, $\tau \sim 2.7 \times 10^5$ s) exhibits a faster charge loss speed than the one using larger nanocrystals (Ge/Si =3/3 nm, $\tau \sim 4.3 \times 10^5$ s), as shown in Fig. 2(a). This is because stronger quantum confinement effect in smaller nanocrystals lifts the energy levels further and therefore shortens the lifetime of the stored charge as shown in Eq. (5). In Fig. 2(b), the transient capacitances are shown for devices with different heteronanocrystal sizes. Larger nanocrystals result in larger capacitance, which is owed to larger permittivity of Ge and Si than that of silicon oxide, and a fixed thickness sum of Ge, Si, and control oxide in all devices. In addition, the decay speed is slightly different for the devices with different dot sizes. For example, the times to decrease the relative capacitance to 80% of the original value are found to be 1.4×10^6 and 1.0×10^6 s for the Ge/Si heteronanocrystals of configurations 3/3 nm and 2/2 nm, respectively. These values are quite close to the retention times obtained from charge amount transient process in Fig. 2(a).

For the above transient capacitance investigation, V_g is fixed at zero. This is reasonable as we do not consider small work function difference between the n-type substrate and the aluminum (Al) gate (4.28 eV for Al and 4.24 eV for n-type Si, respectively[24]), which leads to a zero V_{fb} for a neutral device. To obtain ΔV_{th} from the time-dependent ca-

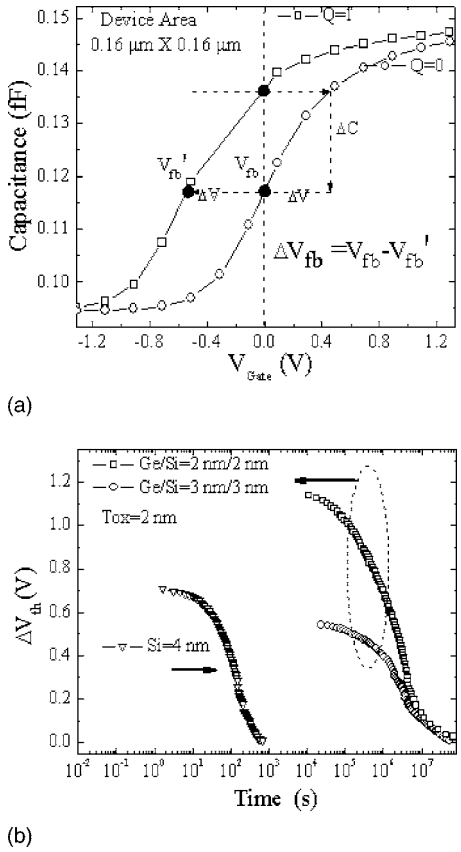

FIG. 3. (a) *C-V* sweep curves for a Ge/Si (2/2 nm) heteronanocrystal memory in the neutral and charged stated. Flatband shift can be obtained from the voltage shift in a constant capacitance mode. (b) ΔV_{fb} as a function of time for memories with Si/Ge heteronanocrystals of 2/2 nm, 3/3 nm, and Si nanocrystals of 4 nm.

pacitances, Fig. 3(a) shows simulated *C-V* sweep curves for charged and neutral Ge/Si (2/2 nm) heteronanocrystal memory devices. The tunneling oxide thickness and dot density are 2 nm and 6×10^{11} cm^{-2}, respectively. Only a voltage shift without any observable deformation of the curve shape is observed between curves. This suggests that with a voltage shift operation, the curve for a charged memory device can match that for a neutral device (reference curve). As a matter of fact, this voltage shift amount is the flatband voltage shift caused by the charge in the nanocrystals. By repeating this operation at different times, the time-dependent ΔV_{fb} can be achieved in a time domain.

In Fig. 3(b), flatband voltage shift ΔV_{fb} as a function of time is shown where the tunneling oxide is fixed at 2 nm and the Ge/Si nanocrystal size is 4 nm (Ge/Si=2/2 nm) and 6 nm (Ge/Si=3/3 nm), respectively. Since larger heteronanocrystals (6 nm) result in a larger capacitance between control gate and heteronanocrystals as a result of thinner effective control oxide, ΔV_{fb} is accordingly smaller (0.54 V). However, it takes 2.8×10^5 s for the memory with Ge/Si =2/2 nm to decrease from 1.1 to 0.90 V (a decline of 20%). To reach the same percentage of decay, the memory with Ge/Si=3/3 nm takes longer time of 6×10^5 s. This indicates indeed a faster charge loss for the memory with smaller heteronanocrystals, which is consistent with the results inferred from Figs. 2(a) and 2(b), since ΔV_{fb} is proportional to the charge amount in the nanocrystal.[1] The advantage of Ge/Si heteronanocrystals over Si nanocrystals is inferred in Fig. 3(b), where a memory with 4 nm Si nanocrystals is compared with a memory with Ge/Si=2/2 nm. ΔV_{fb} drops 20% within 39 s for the device with Si nanocrystals only. In the Ge/Si (2/2 nm) heteronanocrystal device, an improvement factor of about 7.2×10^3 in the retention time has been achieved.

IV. SUMMARY

Transient capacitances of Ge/Si heteronanocrystal memories are investigated numerically. The results show that the transient capacitance exhibits a slower decay, namely, longer retention, for Ge/Si heteronanocrystal memories compared to a Si nanocrystal memory. Larger heteronanocrystal leads to longer retention, larger device capacitance, and smaller flatband voltage shift.

ACKNOWLEDGMENTS

The authors acknowledge the financial and program support of the Microelectronics Advanced Research Corporation (MARCO) and its Focus Center on Function Engineered NanoArchitectonics (FENA).

[1] S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, A. Hartstein, E. F. Crabbe, and K. Chan, Appl. Phys. Lett. **68**, 1377 (1996).
[2] L. Guo, E. Leobandung, and S. Y. Chou, Appl. Phys. Lett. **70**, 850 (1997).
[3] Y. Shi, K. Saito, H. Ishikuro, and T. Hiramoto, J. Appl. Phys. **84**, 2358 (1998).
[4] I. Kim, S. Han, K. Han, J. Lee, and H. Shin, IEEE Electron Device Lett. **20**, 630 (1999).
[5] Z. T. Liu, C. H. Lee, W. Narayanan, G. Pei, and E. C. Kan, IEEE Electron Device Lett. **24**, 345 (2003).
[6] M. She and T. J. King, IEEE Trans. Electron Devices **50**, 1934 (2003).
[7] K. Han, I. Kim, and H. Shin, IEEE Trans. Electron Devices **48**, 874 (2001).
[8] M. Saitoh, E. Nagata, and T. Hiramoto, Tech. Dig. - Int. Electron Devices Meet. 181 (2002).
[9] M. Saitoh, E. Nagata, and T. Hiramoto, Appl. Phys. Lett. **82**, 1787 (2003).
[10] A. Wahl, H. Silva, A. Gokirmak, A. Kumar, J. J. Welser, and S. Tiwari, Tech. Dig. - Int. Electron Devices Meet. 375 (1999).
[11] P. Dimitrakis *et al.*, Mater. Sci. Eng., B **101**, 14 (2000).
[12] Y. Kim, H. J. Cheong, K. H. Park, T. H. Chung, H. J. Bark, J. Y. Yi, S. H. Bang, and J. H. Cho, Semicond. Sci. Technol. **17**, 1039 (2002).
[13] M. Kanoun, A. Soufi, T. Baron, and F. Mazen, Appl. Phys. Lett. **84**, 5079 (2004).
[14] H. G. Yang, Y. Shi, L. Pu, R. Zhang, B. Shen, P. Han, S. L. Gu, and Y. D. Zheng, Appl. Surf. Sci. **224**, 394 (2004).
[15] Y. Zhu, D. T. Zhao, R. G. Li, and J. L. Liu, J. Appl. Phys. **97**, 034309 (2005).
[16] D. T. Zhao, Y. Zhu, R. G. Li, and J. L. Liu, IEEE Trans. Nanotechnol. **5**, 37 (2006).
[17] Y. Li, F. Qian, J. Xiang, and C. M. Lieber, Mater. Today **9**, 18 (2006).
[18] L. Colombo, R. Resta, and S. Baroni, Phys. Rev. B **44**, 5572 (1991).
[19] L. F. Register, E. Rosenbaum, and K. Yang, Appl. Phys. Lett. **74**, 457 (1999).
[20] K. J. Hebert and E. A. Irene, J. Appl. Phys. **82**, 291 (1997).
[21] J. M. Mohaidat, J. Appl. Phys. **90**, 871 (2001).
[22] S. F. P. Paul and H. Fouckhardt, Phys. Lett. A **286**, 199 (2001).
[23] Z. A. Weinberg, J. Appl. Phys. **53**, 5052 (1982).
[24] J. Singh, *Semiconductor Devices: Basic Principles* (Wiley, New York 2000).