$TiSi_2$/Si heteronanocrystal metal-oxide-semiconductor-field-effect-transistor memory

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$TiSi_2$/Si heteronanocrystals with a density of 5×10^{11} cm^{-2} were formed on a thermally oxidized *p*-type Si substrate by using self-aligned silicide technique. Metal-oxide-semiconductor-field-effect-transistor (MOSFET) memory devices were fabricated using these heteronanocrystals as floating gates. As compared to Si nanocrystal MOSFET memory, $TiSi_2$/Si heteronanocrystal memories exhibit higher charge storage capacity, longer retention, better writing efficiency, less writing saturation, and faster erasing speed. © *2006 American Institute of Physics*.
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Si nanocrystals as discrete charge storage nodes have significantly improved the performance of floating gate memory.[1] It has been found that the existence of defects in Si nanocrystals results in the long retention performance. Nevertheless, this defect-related retention enhancement is not thermally robust.[2] Toward better retention and reliability, numerous attempts have been made using floating nanocrystals, such as double Si nanocrystals,[3] Ge nanocrystals,[4] metal,[5–8] or metal-like[9] nanocrystals, and dielectric nanocrystals (Al_2O_3, HfO_2, Si_4N_3, etc.)[10–12] In principle, the issue of the defect-related storage remains for the dielectric nanocrystals since the defect-induced traps are the only mechanism for charge retention. Charging the defects in the dielectric layers also encounters the erasing saturation, as has been found in silicon-oxide-nitride-oxide-silicon memory devices.[13] A feasible solution to rule out the defect effect is to employ nanocrystals with high density of states, such as metal nanocrystals.[5–8] The drawback of using metal nanocrystals is the metal/oxide reaction during high-temperature processes in device integration, such as source/drain/gate dopant activation. Recently we reported the metal-oxide-semiconductor (MOS) capacitor memory with self-aligned silicide/Si heteronanocrystal floating gate.[14,15] Without degrading the performance in writing and erasing, as compared with a Si nanocrystal capacitor, the MOS device exhibited a significantly improved retention, obtained from capacitance-voltage measurements. Two-terminal MOS capacitor device, however, is not practically applicable for nonvolatile memory technology. Toward this application, it is extremely important to develop three-terminal MOS-field-effect transistor (MOSFET) memories and study their current-voltage characteristics and other device physics.

This letter reports the dynamic performance of MOSFET memory devices with $TiSi_2$/Si heteronanocrystal floating gates, including writing, erasing, and data retention. It has been reported that there is a conduction band discontinuity of 0.57 eV at the $TiSi_2$/Si interface.[16] The tunnel barrier profile changes from uniform to staircase when $TiSi_2$/Si heteronanocrystals replace Si nanocrystals. The formation of an additional quantum well for electrons as a result of band offset enhances data retention characteristics compared with Si nanocrystal memory. In addition, Si barrier layers between the metallic silicide dots and the tunnel oxide minimize segregation of the metal atoms into the tunnel oxide, leading to better device stability over metal nanocrystal memories.

$TiSi_2$/Si heteronanocrystal process is briefly described as follows. Si nanocrystals were deposited using low-pressure chemical vapor deposition (LPCVD) on a *p*-type Si wafer with a 5-nm-thick thermally grown tunnel oxide layer. Then the wafer was immediately transferred into another vacuum chamber for Ti metal deposition (2 nm). A standard silicidation technique is used to form silicide/Si heteronanocrystals.[15] The unreacted Ti in between and on top of heteronanocrystals was selectively removed to form discrete heteronanocrystals. After silicidation, control oxide of about 15 nm was deposited, followed by a 350-nm-thick poly-Si deposition in LPCVD. The polygate and source/drain regions were heavily implanted with phosphorus. Aluminum was used as Ohmic contact material. Memories embedding with both original Si nanocrystals and self-aligned $TiSi_2$/Si heteronanocrystals were fabricated in the same run. The final MOSFET memory devices possess a channel length of 1 μm.

Figure 1(a) shows the atomic force microscope (AFM) image of $TiSi_2$/Si heteronanocrystals on the tunnel oxide. Heteronanocrystal density of about 5×10^{11} cm^{-2} and average base diameter of 13 nm can be obtained. To confirm the formation of heteronanocrystals, selective etching of $TiSi_2$ dots over Si dots was conducted in diluted HF. Figure 1(b) shows the AFM image of the heteronanocrystal sample after etching. Si dots are still visible with slightly smaller size and similar density. Figure 1(c) gives the results of x-ray photoelectron spectroscopy (XPS) analysis for the same heteronanocrystal samples before and after HF etching. For the as-fabricated heteronanocrystal sample, there are two evident peaks (466.1 and 461.1 eV) corresponding to $2P_{1/2}$ and $2P_{3/2}$ states of Ti, respectively.[17,18] These two peaks correspond to titanium silicide and partially oxidized titanium[18] caused by the exposure of the sample to the air. These Ti-related signals

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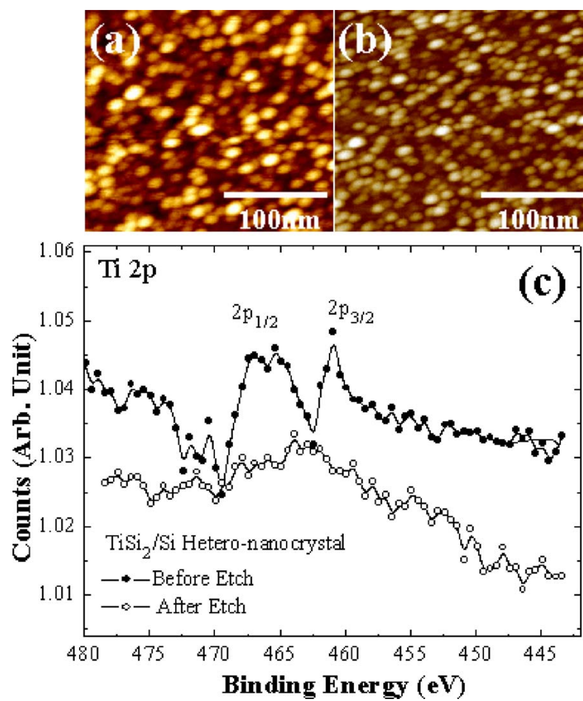

FIG. 1. (Color online) (a) AFM image of the $TiSi_2/Si$ heteronanocrystals of our memory devices. (b) AFM image of the $TiSi_2/Si$ heteronanocrystals after selective etching in diluted HF. Smaller features with similar density as the original $TiSi_2/Si$ heteronanocrystals are the remaining Si dot portions of the heteronanocrystals. (c) XPS spectra of the samples shown in (a) and (b).

disappear after HF etching, which means the removal of the $TiSi_2$ portions of the heteronanocrystals. The combination of XPS and AFM results suggests that $TiSi_2/Si$ heteronanocrystals have been achieved.

Figure 2 shows I_{ds}-V_{gs} characteristics of a $TiSi_2/Si$ heteronanocrystal memory, where I_{ds} is the source-drain current and V_{gs} is the gate voltage, respectively. The drain voltage is fixed at 0.1 V. Positive shift in I_{ds}-V_{gs} curve can be clearly found for the device after a writing operation of 20 V for 1 s, indicating that electrons have been injected into the floating gate. The threshold voltage (V_{th}) is defined as the gate voltage where the channel current reaches 0.1 μA, as is commonly used in industry. Threshold voltage shift (ΔV_{th}), i.e., memory window of about 0.8 V, is obtained.

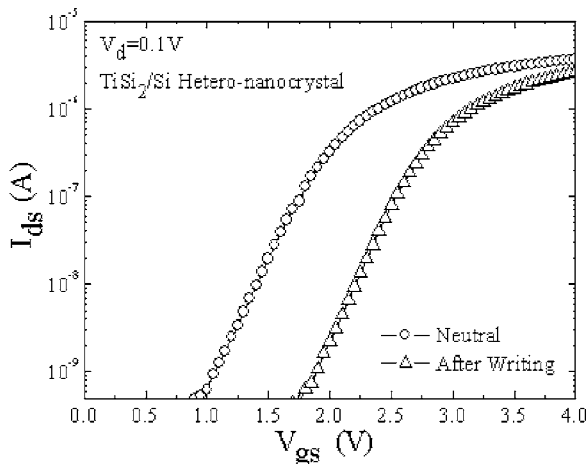

FIG. 2. I_{ds}-V_{gs} curves for the neutral and the programed $TiSi_2/Si$ heteronanocrystal memory. Memory effect is clearly observed.

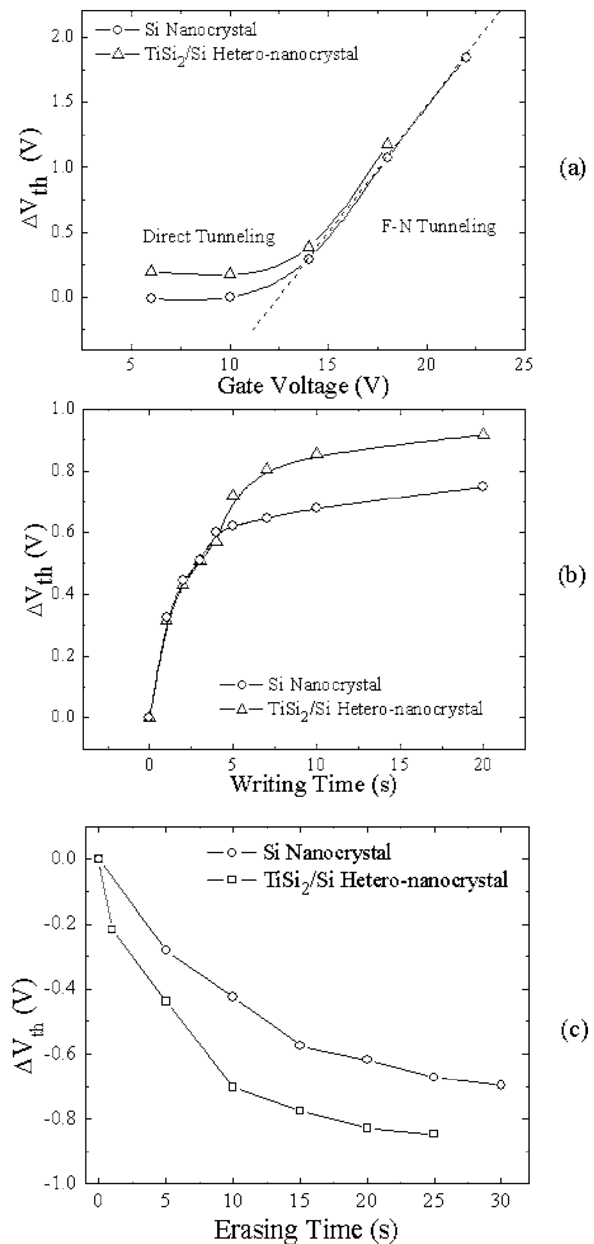

FIG. 3. Threshold voltage shift as a function of (a) writing voltage, (b) writing time, and (c) erasing time, for memories with $TiSi_2/Si$ heteronanocrystal and Si nanocrystal floating gates, respectively.

The memory window is shown in Figs. 3(a) and 3(b), where its dependence on the writing voltage and writing time is plotted, respectively. For the writing voltage dependence, the writing time is fixed at 1 s. Memory window of the device with heteronanocrystals is larger than that of the reference Si nanocrystal memory at the low gate voltages. However, the difference decreases as the gate voltage increases and almost disappears when the writing voltages exceed 14 V. The memory window begins to increase rapidly and linearly when the gate voltage increases beyond 14 V. This is due to the different tunneling mechanisms under low and high voltages. Direct tunneling, although weak, occurs at low electric field, which corresponds to a slow writing. Metallic $TiSi_2$ offers higher density of states and stronger coupling between the heteronanocrystal floating gate and the channel. Therefore the tunneling from the channel to the floating gate occurs more easily, leading to a slightly higher writing efficiency. As the field reaches 7 MV/cm (corresponding to

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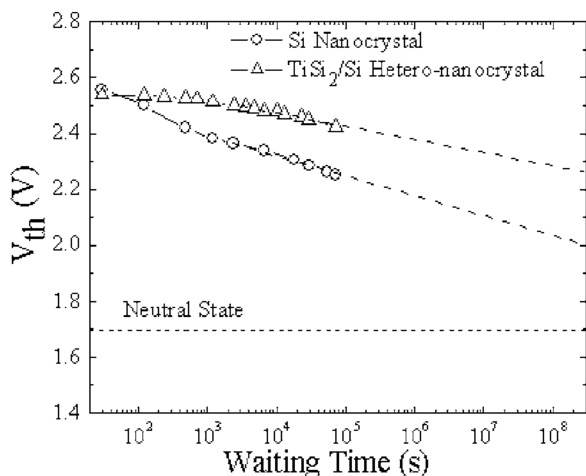

FIG. 4. Retention characteristics of a $TiSi_2/Si$ heteronanocrystal memory and a Si nanocrystal memory.

14 V bias on our devices), Fowler-Nordheim (FN) tunneling begins to dominate the charge injection, thus giving a rapid increase of programming speed. Since FN tunneling occurs when electrons tunnel from the channel, via the triangular tunnel oxide barrier because of high voltage, to the floating nanocrystals, the difference of the band structure near the conduction band edge between the Si nanocrystals and $TiSi_2/Si$ heteronanocrystals is not critical in writing under high voltage. This explains the result that the two memory devices possess the same memory window for the short writing time of 1 s at the high voltage.

Figure 3(b) shows the dependence of memory window on writing time. The writing voltage is fixed at 15 V and writing time is changed from 1 to 20 s. Almost identical trend of memory window for the two devices can be found when the writing time is below 5 s. Beyond 5 s, the writing approaches saturation. The heteronanocrystal memory exhibits a larger saturated memory window. Since writing at 15 V is dominated through FN tunneling, both Si nanocrystal and $TiSi_2/Si$ heteronanocrystal memories have similar writing efficiency, leading to the same memory window trend when the writing time is less than 5 s. However, as the writing time increases, the charge amount in the floating gates increases. The Coulomb blockade effect raises nanocrystals' potential after receiving those electrons and repulses the following electrons from entering the floating gates. Saturation then occurs after a certain injection time for a given gate voltage. $TiSi_2/Si$ heteronanocrystals repulse less strongly the next electrons due to the extremely large effective dielectric constant for metallic material. The resultant characteristic is that $TiSi_2/Si$ heteronanocrystal can store more charges when writing is saturated.

The erasing characteristics are shown in Fig. 3(c) with an erasing voltage of −15 V for both the $TiSi_2/Si$ heteronanocrystal memory and the Si nanocrystal memory. The $TiSi_2/Si$ heteronanocrystal memory exhibits faster erasing speed than the Si nanocrystal memory. This is attributed to higher coupling between the metallic silicide and the channel due to higher density of states.

In Fig. 4, the retention characteristic of the $TiSi_2/Si$ heteronanocrystal memory is much superior to that of Si nanocrystal memory due to the additional barrier from $TiSi_2/Si$ band offset.[14,15] The memory window decay rate for the $TiSi_2/Si$ heteronanocrystal memory is 0.048 V/decade, leading to a 0.56 V window even after ten years (3×10^8 s) as obtained from the elongation line for the decay trend. The Si nanocrystal memory possesses a slightly faster decay rate (0.069 V/decade) after a quick memory window drop in the early retention stage. This decay (0.069 V/decade) is attributed to the detrapping from the deep traps in the Si nanocrystals. These deep traps may have a slightly smaller activation energy (trap depth) than the band offset of $TiSi_2/Si$, which explains the slightly faster emission rate. In the earlier retention stage, charge emission from the Si nanocrystal conduction band and the shallow traps contributes to faster decay than that in $TiSi_2/Si$ heteronanocrystal memory case, leading to a significant charge loss during the first 10^4 s. For the $TiSi_2/Si$ heteronanocrystal memory, since the charges are mainly localized in the additional $SiO_2/TiSi_2/Si$ quantum well region, it does not suffer from faster charge loss in the early retention stage. Therefore it exhibits a dramatically improved retention characteristic.

In summary, we have demonstrated high performance of a MOSFET memory device with self-aligned $TiSi_2/Si$ heteronanocrystal floating gate. Compared with a Si nanocrystal memory, a $TiSi_2/Si$ heteronanocrystal memory exhibits faster writing, weaker writing saturation, faster erasing, and longer retention characteristics. This study suggests that $TiSi_2/Si$ heteronanocrystal memory is a promising candidate to replace flash memory and Si nanocrystal memory for applications toward complementary MOS ultimate limit.

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