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Transient processes in a Ge/Si hetero-nanocrystal p-channel memory

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Abstract

Transient processes of Ge/Si hetero-nanocrystal floating gate memories are simulated numerically. Compared with Si nanocrystal memories, Ge/Si hetero-nanocrystal memories show similar writing and erasing efficiency with a weaker writing saturation and markedly improved retention characteristics.
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1. Introduction

Si nanocrystals (NCs) as discrete storage nodes are very promising to replace conventional continuous metal or poly-Si floating gate in a metal-oxide-semiconductor-field-effect-transistor (MOSFET), offering the advantages of smaller device size, higher programming speed and lower operation voltage [1–5]. As scaling continues to reduce the tunneling oxide thickness for lower operation voltages, the simultaneous realization of a long retention time as well as a high writing/erasing speed is very important, but, challenging. Due to the quantum confinement effect, either the valence band edge (E_v) or the conduction band edge (E_c) of the Si NC is higher than that of the Si substrate, which degrades the retention characteristics as the charge stored in the NC can easily leak back to the substrate. Therefore it is believed that the long charge storage occurs mainly in the defect-related traps instead of in the conduction or valence bands [3,4,6]. However, the defect-related traps are sensitive to operation temperature and also difficult to be controlled in device fabrication. Therefore, good consistency in device performance is not easily achieved, especially for devices containing only several or even one nanocrystal storage node. Recently, Ge/Si hetero-nanocrystals (HNC) were proposed to replace Si NCs as the floating gate [7] for a p-channel memory, using the quantum well formed by control oxide/Ge/Si to confine a hole in a Ge dot region. Since E_v of Ge is lower than that of a Si dot, the hole in retention mode should first be thermally excited to a certain energy level higher than the valence band edge of the substrate before tunneling occurs. Therefore, retention can be markedly improved without sacrificing writing/erasing efficiency.

Although writing/erasing and retention time [7] and threshold voltage shift [8] of a Ge/Si HNC memory have been systematically investigated, research on the dynamic characteristics is still lacking. A Ge/Si HNC memory can behave differently in real operation because both Coulomb blockade effect and quantum confinement effect are different from those in a Si NC memory device. The aim of this work is to reveal the time-dependent dynamic processes in writing/erasing and retention of a Ge/Si hetero-nanocrystal

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(HNC) memory, demonstrating the advantage of a Ge/Si HNC memory over a Si NC memory.

2. Theory and model

In principle, all of the transient processes in this paper are based on a relation as given by:

$$Q(t+\Delta t) = Q(t) \pm I_t \times \Delta t, \tag{1}$$

where Q, t, Δt and I_t are the charge in the nanocrystal, the time, the time step and the transient tunneling current, respectively. The charge in the nanocrystal deforms the electrical potential profile in the device and, thus, influences the band structure and in turn the tunneling current. During each step, the electrical potential is derived by solving Poisson equation using finite difference method with the presence of the charge in the nanocrystal. Based on this potential profile, the tunneling probability is calculated by the transfer matrix method [9,10].

The tunneling current density is given by [11,12]:

$$J = q \int_{E_{\text{shift}} \leqslant E} T(E) f(E) \rho(E) F(E)\, \mathrm{d}E, \tag{2}$$

where $f(E)$ is the impact frequency, $\rho(E)$ the two-dimensional (2D) density of states, $F(E)$ the Fermi–Dirac distribution function and $T(E)$ the tunneling probability obtained from the transfer matrix method, respectively. E_{shift} is the Si valence (for writing process) or conduction band (for erasing process) shift due to the quantum confinement effect from the small size of the nanocrystal. The impact frequency reads [11]:

$$f(E) = 0.6 \times \frac{2q}{\left(3\pi\hbar m_{\text{Si},\perp}\right)^{1/3}} \left(\frac{\varepsilon_{\text{ox}} F_{\text{ox}}}{\varepsilon_{\text{Si}}}\right)^{2/3}, \tag{3}$$

where $\hbar$, $m_{\text{Si},\perp}$, ε_{ox}, F_{ox}, and ε_{Si} are the reduced Planck's constant, the hole (or electron) effective mass perpendicular to the substrate, the dielectric constant of SiO_2, the surface electric field in the SiO_2 layer, and the Si dielectric constant, respectively. The density of states for a 2D confined hole or electron gas is [11]:

$$\rho(E) = \frac{m_{\text{Si},//}}{\pi\hbar^2}, \tag{4}$$

where $m_{\text{Si},//}$ is the hole or electron effective mass in the confined plane of the accumulation or the inversion layer of the substrate. The surface field in the oxide layer F_{ox} is derived by iteratively solving Poisson equation with a finite difference technique. Only the electrons or holes in the accumulation or inversion layer with energy higher than the conduction or valence band edge can tunnel to the nanocrystals.

The retention time (τ) of the charge storage is derived from the following expression:

$$\tau = \frac{1}{\sum_{i=n}^{\infty} \exp\left(\frac{-(E_i - E_0)}{k_B T}\right) f(E_i) T(E_i)}, \tag{5}$$

where E_i and E_0 are the ith excited state and ground state (for holes) in the hetero-nanocrystal respectively, and k_B is Boltzmann's constant. The integer number, 'n', is the quantum number from which the wave function of the hole spreads over both Ge and Si regions of the hetero-nanocrystal. Note E_n is automatically greater than E_v of Si. Thus, the states with quantum number greater than 'n' can tunnel to the Si substrate. The term $\exp(\frac{-(E_i-E_0)}{k_B T})$ in Eq. (5) represents the de-trapping coefficient, since a hole confined in a Ge dot region should be first thermally activated to the nth excited state before it can tunnel to the substrate. This process is very similar to the de-trapping process described in the paper of She and King [6]. The eigen energy levels and corresponding wave functions are calculated using an improved shooting method [13] with the effective mass approximation model. Based on the eigen energies the Weinberg's impact frequency $f(E_i)$ can be written as [12]:

$$f(E_i) = \frac{E_i - E_0}{h}, \tag{6}$$

where h is Planck's constant. For all the calculations, the control oxide is fixed at 5 nm so that tunneling through control oxide can be disregarded since tunneling probability strongly depends on the barrier thickness.

The source-to-drain current (I_{DS}) calculation is based on a linear model using a small drain-to-source voltage, V_{DS}:

$$I_{DS} = -\mu_{\text{Surf}} Q_{\text{Surf}} V_{DS} \frac{W}{L}, \tag{7}$$

where μ_{Surf}, Q_{Surf}, W and L are the carrier mobility in the inversion layer, charge in the inversion layer, the channel width and the channel length, respectively. Q_{Surf} is obtained using

$$Q_{\text{Surf}} = \varepsilon_{\text{ox}} F_{\text{ox}} WL. \tag{8}$$

In our simulations, the channel length and width are assumed to be both 1 μm, and the mobility μ_{Surf} is taken as 400 $\text{cm}^2/\text{V s}$. V_{DS} is chosen as 0.01 V which is sufficiently small so that the potential from the control gate voltage is not deformed by it.

The threshold voltage shift of the device is defined as the gate voltage when the hole density near the interface of the tunneling oxide/substrate reaches the value of the density deep in the substrate. The shift is then derived by comparing the two threshold voltages for a charged and uncharged memory, respectively.

3. Results and discussion

The writing transient processes at −4 and −6 V are shown in Fig. 1 for (a) the current density, (b) sheet charge density in the floating gates (Ge/Si = 5 nm/3 nm and Si = 8 nm) and (c) the transient threshold voltage shift (ΔV_{th}) of the devices. The dot density is kept as a constant of $6 \times 10^{11}\ \text{cm}^{-2}$. The tunneling oxide thickness (T_{ox}) is 2.0 nm. As writing continues, the injection efficiency

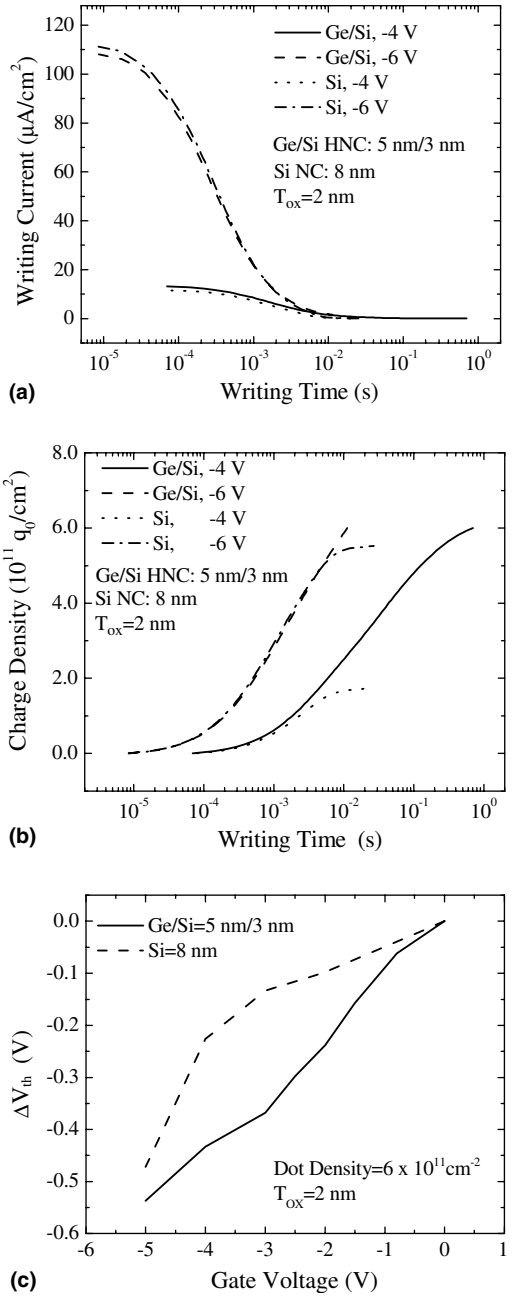

Fig. 1. Writing transient for Ge/Si hetero-nanocrystal memory and Si nanocrystal memory. (a) The writing current as a function of time, (b) the charge density in floating gate as a function of writing time, and (c) the threshold voltage shift as a function of gate voltage.

decreases due to the repulsion between the stored charge and the incoming charge, exhibiting a saturation feature in the writing curves for both Ge/Si HNC and Si NC memory devices. Fig. 1(a) indicates no evident difference between the writing currents for the Ge/Si HNC device and the Si NC device. However, as shown in Fig. 1(b), writing saturation for the Ge/Si HNC device is weaker than that of the Si dot device. This is attributed to the difference of the charging energy between a Si dot and a Ge/Si HNC of the same size. Since the charging energy for a NC is proportional to the reciprocal of its self-capacitance, and a Ge/Si hetero-dot possesses a larger self-capacitance than a Si dot of the same size due to the higher dielectric constant of Ge than Si, the charging energy for a Ge/Si HNC is higher than for a Si NC. The self-regulated writing process limits the charge amount that can be injected to the NC floating gate. In other words, the maximum threshold voltage shift (ΔV_{th}) due to the stored charge amount is self-limited at a given writing voltage. The ultimate value of ΔV_{th} as a function of writing voltage is shown in Fig. 1(c). One observes that with lower writing voltage, the Si dot device shows a lower ΔV_{th} value than its Ge/Si hetero-dot counterpart. However, the Ge/Si HNC memory exhibits a ΔV_{th} value closer to that for a Si NC memory as the gate voltage increases. This is because writing saturation is stronger for Si dot memory than Ge/Si hetero-dot memory, which limits the charge (hole) amount in the NCs at lower writing voltage. Since ΔV_{th} is proportional to the charge stored in the floating gate, larger charge quantity leads to larger ΔV_{th}, as shown in Fig. 1(c).

The effect of the size of the Ge component on the writing process is shown in Fig. 2, where the transient threshold voltage shift is given as a function of time. It is found that a faster ΔV_{th} increase can be achieved by using smaller Ge dots on top of Si dots. Our calculation has shown that ΔV_{th} for a Ge/Si HNC memory device depends quite significantly on the sizes of the Ge dot and the Si dot [8]. Smaller Ge dots introduce larger ΔV_{th} [8], i.e., larger screening effect from the trapped charge on the gate voltage, which consequently depresses the writing process more remarkably than the cases of larger Ge dots.

The comparison of the erasing processes between a Ge/Si HNC memory and a Si NC memory is shown in Fig. 3(a) and (b). The tunneling oxide is fixed at 2.0 nm for both memories. For simplicity, it is assumed that each dot is occupied by one hole only. The nominal size of the dot is kept at 8 nm. Although the initial erasing currents are different for a Ge/Si HNC memory and a Si NC memory as shown in Fig. 3(a), it is clear that the erasures for Si NC

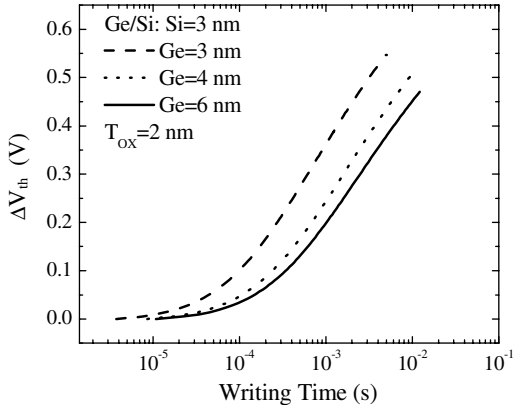

Fig. 2. Threshold voltage shift evolution during writing for a Ge/Si hetero-nanocrystal memory. The writing voltage is –6 V and the tunneling oxide is fixed at 2 nm.

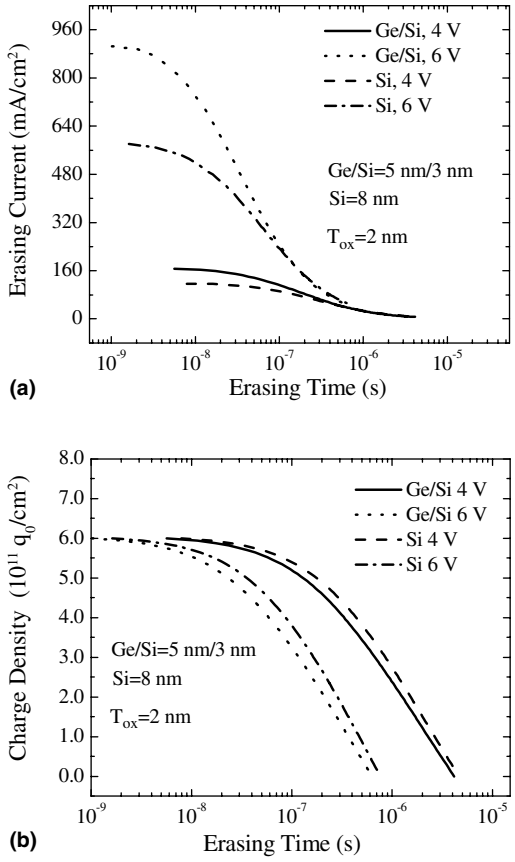

Fig. 3. Comparison of the erasing transients between Ge/Si heteronanocrystal and Si nanocrystal memory devices. (a) The transient erasing current at 4 and 6 V, respectively and (b) charge density in floating gate as a function of erasing time.

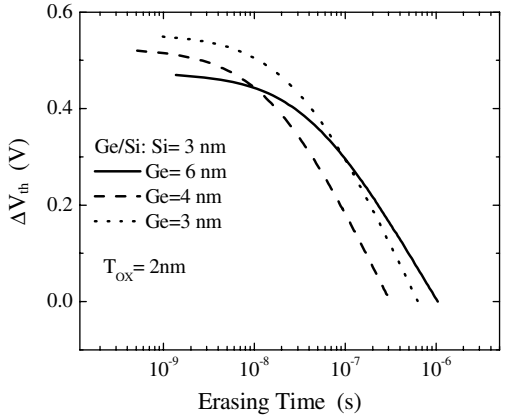

Fig. 4. Threshold voltage shift evolution during erasing Ge/Si heteronanocrystal memories with different Ge dot sizes. The erasing voltage is 6 V and the tunneling oxide is fixed at 2 nm.

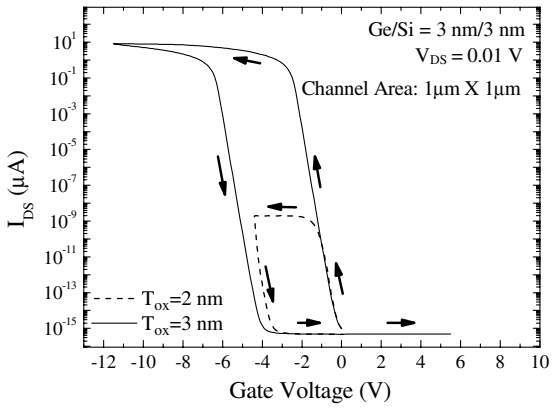

Fig. 5. Two simulated voltage sweeping measurements of source-to-drain current as a function of the gate voltage. The tunneling oxide thicknesses for the two curves are 2 and 3 nm, respectively. The Ge/Si dot size is 3 nm/3 nm. The sweep speed is 0.2 V/s.

and Ge/Si HNC devices are almost the same at the same erasing voltage in Fig. 3(b). This is due to the fact that the charge quantity in the floating gate is the time integral of current. Therefore, the initial higher current does not contribute significantly to the charge density in the floating gate. It can also be found in Fig. 3(b) that when the erasing voltage decreases from 6 to 4 V, the erasing speed decreases accordingly by a factor of about six. The transient ΔV_{th} during erasure at 6 V for a Ge/Si HNC memory with different Ge dot size is shown in Fig. 4, where no simple trend for erasing a Ge/Si HNC memory can be found. This is due to the combination of quantum mechanical effect and charge density-dependent potential distortion. Since smaller dot leads to stronger quantum confinement and Coulomb blockade effect, which raise the ground state energy and hinder electron current from substrate to nanocrystals. In the meantime, smaller dot possesses higher charge density, which distorts the potential strongly and favors faster erasing. The competition of these two factors leads to an optimized erasing condition.

Fig. 5 shows the simulated gate voltage sweeping measurement. The source–drain current (I_{DS}) is recorded during the gate voltage sweep with a sweep speed 0.2 V/s. Two memory devices with different tunneling oxide thicknesses (2 and 3 nm, respectively) are investigated. Clear hysteresis loops can be found, indicating the memory effect. It is interesting to note that the saturated source–drain current in the case of a thinner (2 nm) tunneling oxide is much lower than the case in which a thicker (3 nm) tunneling oxide is used. This originates from the rapid charging through a thinner tunneling oxide. The charge in the floating gate accumulates very fast and consequently strongly screens the gate potential so that the potential in the channel does not increase any longer. Therefore, the charge density and the channel current do not respond to the gate voltage increase.

The retention characteristics for a Ge/Si HNC and a Si NC memory device are shown in Fig. 6, where the tunneling oxide is fixed at 2.0 nm for all the devices involved. The initial hole number is assumed to be one in each nanocrystal. One observes that the retention time for a smaller Ge/Si HNC is shorter than that for a larger HNC, which is attributed to the quantum confinement effect that contributes more for the device with smaller dots. It is notable that

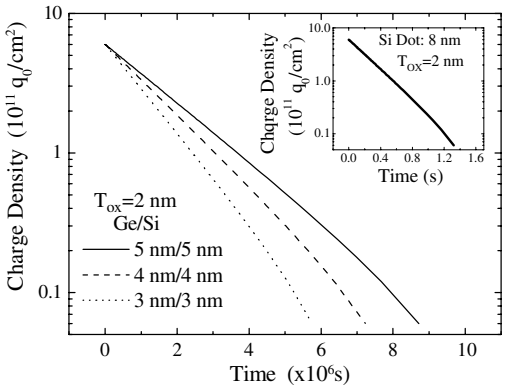

Fig. 6. Charge retention transients of Ge/Si hetero-nanocrystal memories with different Ge/Si dot sizes. The inset is the time-dependent charge in the Si nanocrystal memory. The tunneling oxide is 2.0 nm for all the devices.

a defect-free Si NC memory with the same dot size (8 nm) and tunneling oxide thickness possess an extremely short retention time, in the order of 1 s, as shown in the inset of Fig. 6. However, the retention is in the order of 10^6 s for a Ge/Si HNC memory, despite influence of the dot size, showing the evident advantage of using Ge/Si HNCs to replace Si NCs for future flash memory.

4. Conclusion

The dynamic transient processes for Ge/Si hetero-nanocrystal flash memory devices are simulated. The influences of Ge/Si dot size, tunneling oxide thickness and gate voltage on writing, erasing and retention transient characteristics are investigated. Compared with a Si nanocrystal memory, a Ge/Si hetero-nanocrystal improves the retention characteristics dramatically without significantly influencing the writing/erasing speed. A Ge/Si hetero-nanocrystal memory shows a weaker writing saturation feature than a Si nanocrystal memory. Almost exactly the same erasure performance is found for Ge/Si hetero-nanocrystal memory and Si nanocrystal memory if the erasing voltage is the same. Therefore, a Ge/Si hetero-nanocrystal memory can replace a Si nanocrystal memory and the scaling-down process of flash memory can be continued.

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References

[1] Tiwari S, Rana F, Chan K, Hanafi H, Chan W, Buchanan D. Appl Phys Lett 1996;68:1377–9.
[2] Nakajima A, Futatsugi T, Kosemura K, Fukano T, Yokoyama N. Appl Phys Lett 1997;70:1742–4.
[3] Shi Y, Saito K, Ishikuro H, Hiramoto T. J Appl Phys 1998;84:2358–60.
[4] Shi Y, Saito K, Ishikuro H, Hiramoto T. Jpn J Appl Phys 1999;38:2453–6.
[5] Saitoh M, Nagata E, Hiramoto T. Appl Phys Lett 2003;82:1787–9.
[6] She M, King TJ. IEEE Trans Electron Dev 2003;50:1934–40.
[7] Yang HG, Shi Y, Pu L, Gu SL, Shen B, Han P, et al. Microelectron J 2003;34:71–5.
[8] Zhu Y, Zhao DT, Li RG, Liu JL. J Appl Phys 2005;97:034309.
[9] Ando Y, Itoh T. J Appl Phys 1987;61:1497–502.
[10] Yang WW, Cheng XH, Xing YM, Li WJ, Yu YH. J Appl Phys 2003;94:4032–5.
[11] Register LF, Rosenbaum E, Yang K. Appl Phys Lett 1999;74:457–9.
[12] Weinberg ZA. J Appl Phys 1982;53:5052–6.
[13] Paul SFP, Fouckhardt H. Phys Lett A 2001;286:199–204.