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Fabrication of Silicon Quantum Wires by Conventional Silicon Processing*

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Abstract

Ultra fine silicon quantum wires with the Si/SiO_2 heterointerface have been fabricated successfully by using reactive ion etching, anisotropic wet chemical etching and subsequent thermal oxidation. The cross-sectional image of scanning electron microscope shows the silicon quantum wires of high quality with the linewidth down to 20nm. The present method has many remarkable advantages, which is important to the study of low-dimension quantum physics and devices.

Key words: Quantum wire, Silicon, Silicon dioxide, Silicon technique

1. Introduction

In the coming decade, today's silicon integrated circuit technology will develop into nanometer linewidth dimension, that is, from microelectronics into nanoelectronics. The silicon wire with the linewidth less than 100 nm is commonly called as silicon quantum wire (SQW). Carriers (electrons or holes) confined in such nanostructures have only one freedom of motion in the dimension along a wire and no freedom in other two dimensions. It would lead to a range of quantum effect phenomena and changing the mode of device operation. As the base of nanoelectronics, obviously, SQWs will play the dominant role in ultra large scale integrations (ULSI) and high performance quantum effect devices[1-3]. Furthermore, because the band structures of these silicon nanostructures are different from those of bulk silicons, so they can obtain new and novel optical properties and thus can be applied to develop silicon optoelectronic integrated devices[4,5]. Silicon nanostructure materials are the most exciting desirables for the study of the basic science and the potential technology of semiconductors. However, due to the fact that it is quite difficult to make silicon single crystal nanostructures, very few attempts have been made in the fabrication of SQW previously. At the present stage, it is requested urgently to develop novel fabrication techniques of high-quality SQWs.

2. Fabrication

In this letter, we report briefly on a capable fabrication method for the SQWs with the Si/SiO_2 heterointerface using anisotropic wet chemical etching, thermal oxidation, and low-temperature silicon epitaxy technique. With this process we ultimately obtained SQWs of high quality with the linewidth down to 20 nm and their scanning electron micrographs. Fig. 1 shows a schematic of SQWs fabricated in this work. An array of SQWs lie on the silicon substrate, where SQWs are embedded in a SiO_2 layer. This kind array of the SQWs is very applicable to the study of silicon quantum physics and devices.

All SQWs were fabricated on (100) silicon wafer by conventional silicon integrated circuit processing. First, a 100 nm thermally oxidized SiO_2 layer was grown acting as a mask for anisotropic wet chemical etching. Then, line-and-space patterns along the

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[011] direction were formed by conventional lithography technique. Next, 350-nm-deep trenches were generated in the substrate by using reactive ion etching. After removing the photoresist, the substrate was dipped in the strong anisotropic etchant using ethylendiomine-pyrocatechol-water solutions to form silicon wires having an upside down triangle cross-section on the top of saw tooth structure with (111) facets. Subsequently, the silicon wires were thermally oxidized at high temperature for some time in order to isolate the silicon wires from the substrate. Finally, mid-temperature process of the thermal oxidation was used to thin the dimension of the silicon wires, and the ultra fine SQWs were obtained.

Fig. 2 shows the cross-section SEM micrographs of the SQWs. Prior to the thermal oxidation process, silicon wires with upside down triangle cross section are prepared, as seen from Fig. 2(a). Fig. 2(b) presents a ultra fine SQW embedded in the SiO_2 layer after thin processing by therma oxidation. Here, the linewidth of the SQV is about 20nm. The thermal oxidation characteristic of the silicon wires is also investigated. As one of the most remarkable advantages, the dimension of the SQW can b controlled excellently by changing the temperature of the thermal oxidation proces due to the self-limiting oxidation effect o silicon nanostructure materials.

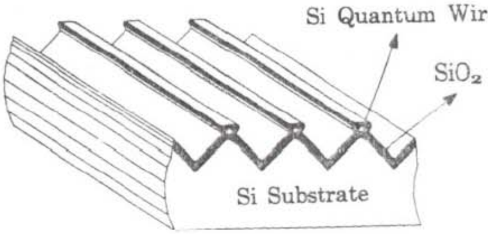

Fig 1. Schematic of SQW array with the Si/SiO_2 heterointerface

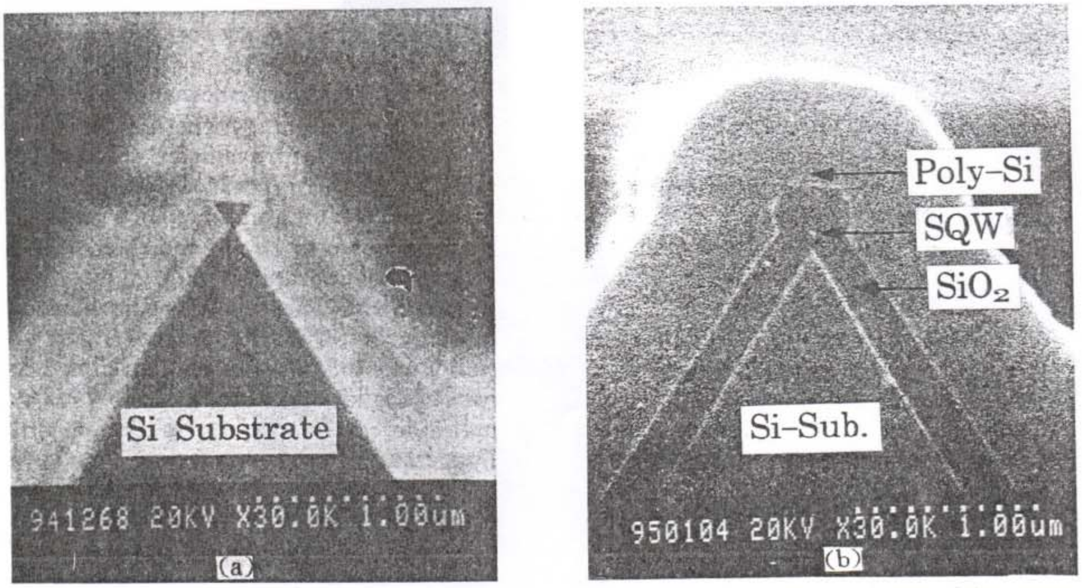

Fig 2. Cross-sectional images of SEM
(a) As-etched silicon wire with upside-down triangle; (b) Thinned SQW with the linewidth of ~20 nm

3. Advantages

Comparing with the methods reported previously, the present one offers many remarkable advantages: (1) Defect-free SQW made of high quality single crystal silicon can be realized by conventional silicon processing, furthermore, the smooth Si/SiO_2 heterointerface of high quality is achieved by thermal oxidation; (2) The wide-gap SiO_2 acts as high potential barrier, and carriers (electrons or holes) are confined completely in the quantum wire; (3) The dimensions of SQW can be controlled precisely by selecting the temperature of the thermal oxidation process; (4) The definite position and dimension of the SQW, as well as large-area array, are very applicable for the study of physics and devices; (5) The present method would provide a promising approach for shrinking device size down to 100 nm linewidth; (6) It would allow to fabricated silicon quantum effect devices and conventional integrated circuit devices on a same silicon chip.

4. Conclusion

In conclusion, we have successfully fabricated ultra fine SQWs with the Si/SiO_2 heterointerface mainly utilizing anisotropic wet chemical etching, subsequent thermal oxidation and low temperature silicon epitaxy technique. It is found that the dimensions of SQW can be controlled precisely by thermal oxidation process. The SQWs are well confirmed by scanning electron microscope imaging. This method is important to the study of low-dimension silicon quantum physics and devices.

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