Self-aligned $TiSi_2/Si$ heteronanocrystal nonvolatile memory

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The titanium silicide/silicon ($TiSi_2/Si$) heteronanocrystals are fabricated on SiO_2 thin films. The metal-oxide-semiconductor structure embedding the $TiSi_2/Si$ heteronanocrystals shows superior performance over the Si dot device. The charge loss rate in the $TiSi_2/Si$ heteronanocrystal device is 7.5 times less than that of the Si dot device. It is also found that the $TiSi_2/Si$ heteronanocrystal device has wider memory window than the Si dot counterpart. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2183815]

Due to the discrete nature, Si nanocrystals in a metal-oxide-semiconductor (MOS) field-effect-transistor structure as the floating gates possess a promising future and have been extensively investigated since it was pioneered by Tiwari *et al.*[1] Besides Si nanocrystals, tremendous effort has also been made to exploit new kinds of nanocrystal floating gate, such as Ge nanocrystals,[2] metal,[3–6] or metallike[7] dot and dielectric nanocrystals (Al_2O_3, HfO_2, Si_4N_3, etc.).[8–10] Intrinsically, semiconductor nanocrystals encounter the issue that the large amount of defect-induced charge traps play important roles in the memory mechanism due to the relatively small density of states of the nanocrystals. Therefore, the annealing treatment of the device can dramatically change the device performance, which in other words means the thermal instability of the device. The situation remains for the dielectric nanocrystals since the defect-induced traps are now the only mechanism for charge retention. Furthermore, the higher defect levels also induce the erasing saturation as has been found in the silicon-oxide-nitride-oxide-silicon memory device.[11] A feasible solution to rule out the defect effect is to employ nanocrystals with high density of states, such as metal nanocrystals.[3–6] One concern of using some metal nanocrystals is the possible reaction between the oxide and the metal during the annealing processes for the metal dot formation. To solve this issue, recently the metal-like TiN nanocrystals have been reported[7] which exhibits good thermal ability of the nanocrystals.

In this letter, we report the MOS memory device using $TiSi_2/Si$ heteronanocrystals as the floating gates. Due to the self-alignment nature of the $TiSi_2$ on Si, the $TiSi_2/Si$ heteronanocrystals can be readily fabricated based on Si nanocrystals. The work function difference between $TiSi_2$ and Si and additional barrier of Si for charges in $TiSi_2$ help the data retention and rule out the effect from defect-related shallower-level traps inside the nanocrystals and at the interface of nanocrystal/oxide.

A chemically cleaned 4 in. p-type Si wafer with doping concentration of 5×10^{15} cm^{-3} is oxidized at 1000 °C for 4 min that results in a thermal oxide layer with the thickness of about 6 nm. The $TiSi_2/Si$ heteronanocrystals were fabricated via a two-step self-aligned silicide technique. First, the Si nanocrystals of about 20 nm in base diameters were grown on the 6 nm tunneling oxide barrier layer in a low pressure chemical vapor deposition (CVD) chamber at 600 °C for 25 s with the SiH_4 pressure of 200 mTorr. The dot density is about 10^{10} cm^{-2}. In the second step, a 5 nm thick metal Ti was deposited onto the sample and the first annealing was performed subsequently at the temperature of 750 °C for 3 min in nitrogen. At such relatively low-temperature condition, the reaction between Ti and SiO_2 is minimized,[12] and Ti reacts with Si only to form the high-resistive C-49 phased $TiSi_2$ (Ref. 13) on top of each Si dot. The unreacted Ti metal on top of nanocrystals as well as in between nanocrystals was removed in selective etchant (NH_4OH: H_2O_2: H_2O=1:1:5). Discrete $TiSi_2/Si$ heteronanocrystals with the same density as original Si dots were formed in this stage. The second annealing was performed also in nitrogen gas at 880 °C for 1 min after the metal removal to convert high-resistive C-49 $TiSi_2$ to low-resistive C-54 $TiSi_2$.[13] Due to fine-line effect,[14] only portion of C-49 $TiSi_2$ may be converted as a result of small dimension of original Si dots. Nevertheless, it is not critical to use low-resistive $TiSi_2$ phase for floating gate of memory as the work function difference between Si and $TiSi_2$ is the dominant factor to enhance the device performance. The sample was then capped with the control oxide of about 50 nm in a low-temperature oxide CVD furnace. Aluminum electrodes on back and front side of the sample were finally deposited and patterned to size of 0.45×0.2 mm^2. The resultant nanocrystals were characterized with scanning electron microscope (SEM) for the surface morphology and electron energy dispersive x-ray (EDX) spectroscope for the composition, respectively. The memory characteristics were investigated by Agilent 4284A LCR meter at room temperature. The memory window and time-dependent transient capacitance (C-t) were measured with capacitance-voltage (C-V) sweep at 1 MHz and constant voltage mode. Time-dependent flat-band voltage shift (ΔV_{fb}-t) was deduced with LABVIEW code at constant capacitance mode.

Figure 1 shows the SEM images and EDX results of the Si nanocrystals [Fig. 1(a)], the $TiSi_2/Si$ heteronanocrystals on SiO_2 tunneling barrier layer [Fig. 1(b)], and Si dot after $TiSi_2$ removal with 10% HF dipping [Fig. 1(c)]. One finds the dot density does not vary while the average dot size increases from ~20 [Fig. 1(a)] to 30 nm [Fig. 1(b)], indicating the excellent self-aligned growth of $TiSi_2$ on Si dots only. The EDX result in Fig. 1(a) resolves Si and oxygen signals for Si nanocrystals on tunneling oxide. Besides these signals, the EDX result shows indeed the signal peak of Ti element

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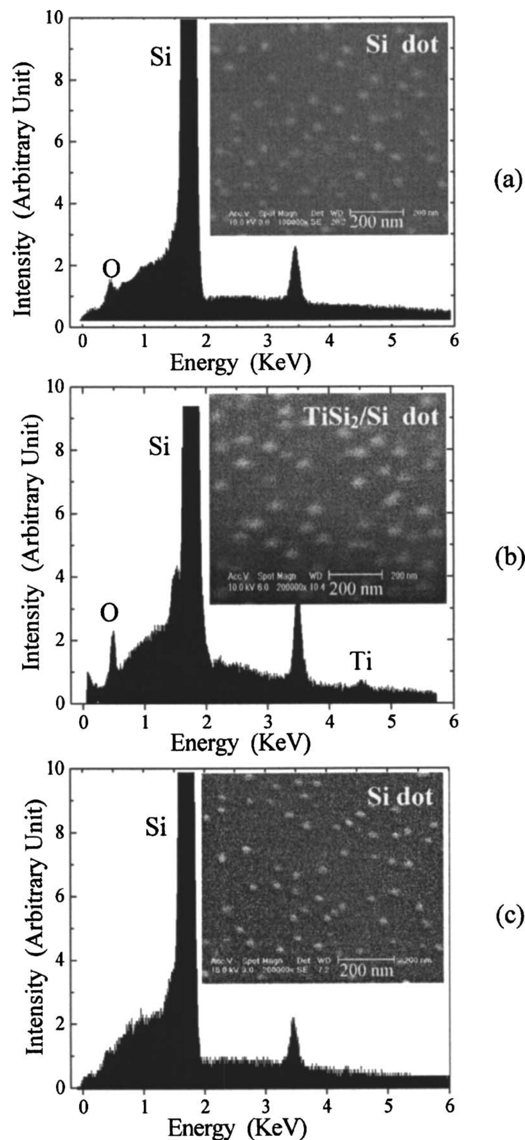

FIG. 1. The characterization of the fabricated $TiSi_2/Si$ heteronanocrystals on SiO_2 thin film. SEM images and corresponding EDX spectra of Si nanocrystals (a), $TiSi_2/Si$ heteronanocrystals (b), and Si nanocrystals after $TiSi_2$ removal with 10% HF (c).

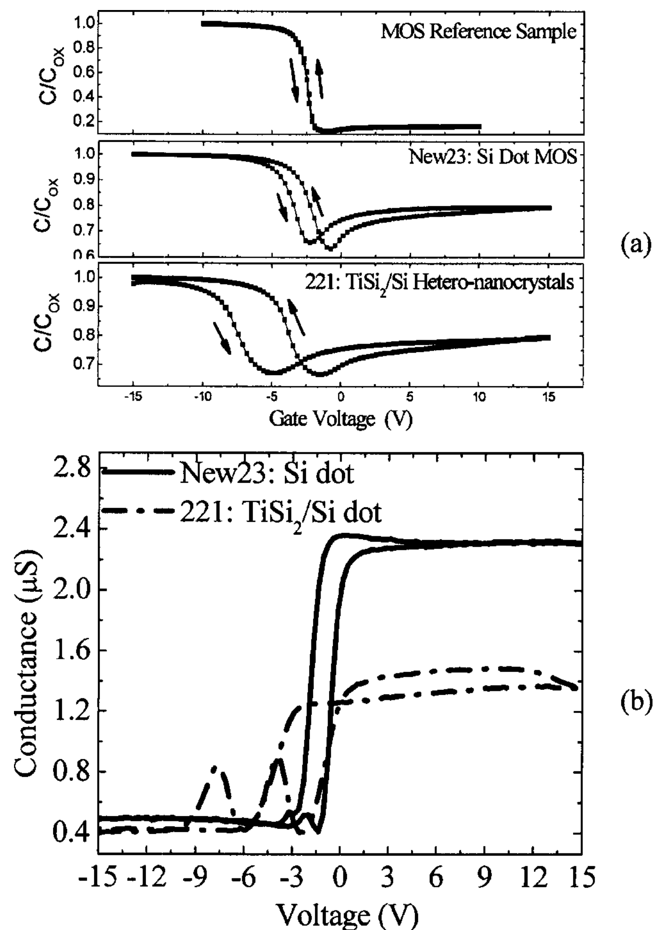

FIG. 2. *C-V* (a) and *G-V* (b) measurement results for the MOS capacitors containing $TiSi_2/Si$ heteronanocrystals and Si nanocrystals only, respectively.

around 4.51 keV from $TiSi_2/Si$ heteronanocrystals, which confirms silicide formation [Fig. 1(b)]. Since the EDX signal penetration depth is of the order of 1 μm, the Ti signal from the hetero-nanocrystals is fairly weaker than the Si signal. To confirm the nanocrystals observed in Fig. 1(b) are $TiSi_2/Si$ heterostructures rather than $TiSi_2$ nanocrystals only, diluted HF etching was used to remove $TiSi_2$. The SEM image in Fig. 1(c) suggests that the observed smaller dots should be Si dots as no Ti signal is detected in the EDX experiment. Since diluted HF also etches SiO_2, negligible oxygen signal is detected. The peaks around 1.55 keV and 3.45 keV observed in all samples are from Si substrate.

The memory effects characterized by *C-V* for the reference MOS, the Si dot MOS and the $TiSi_2/Si$ heterodot MOS memories are shown in Fig. 2(a), where the hysteresis feature can be found only for the Si dot MOS and the heterodot MOS capacitors after the gate voltage swept from accumulation region to inversion region and then swept back. No *C-V* hysteresis is found for the MOS capacitor with only tunneling oxide, but without control oxide and nanocrystals embedded. Smaller minimum C/C_{ox} at high positive voltages in the reference MOS sample compared with the other two memory devices is a result of its thinner dielectric layer. The conductance-voltage (*G-V*) curves during the gate voltage sweep are shown in Fig. 2(b), where the similar hysteresis can be observed for both the Si dot MOS and the heterodot MOS devices. The width of the hysteresis is defined here as the memory window which indicates how obviously the flat-band voltage (V_{fb}) or the threshold voltage (V_{th}) responds to the charge injected to the nanocrystals. There are two evident differences between the Si dot MOS and the heterodot MOS in their *C-V* and *G-V* curves. First, the memory window for the $TiSi_2/Si$ heterodot MOS memory is much larger than that of the Si dot MOS memory. Second, for the heterodot MOS capacitor, the flat-band in the *C-V* flank (from the accumulation region to inversion region) is shifted from the neutral device *C-V* curve more toward negative voltage compared with the Si dot MOS device. Since the control oxide of the two memory devices was obtained in the furnace process at the same time, relatively similar amount of fixed positive charges in the oxide and oxide thickness can be expected, which shift the *C-V* curves to the negative direction. Nevertheless, the ability of storing more charge in the $TiSi_2/Si$ heteronanocrystal device leads to wider memory window as it is proportional to the charge quantity in the floating dots. The *C-V* stretchouts in Fig. 2(a) for Si nanocrystal device and $TiSi_2/Si$ heteronanocrystal device indicate

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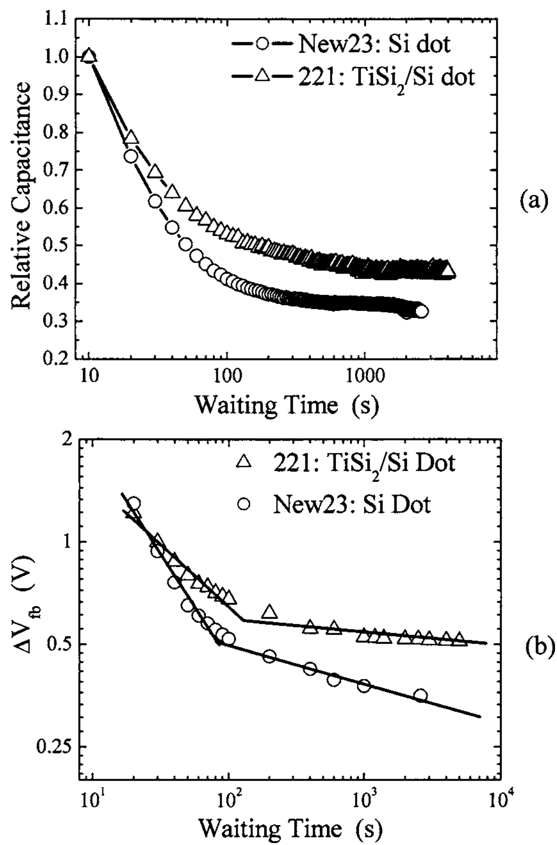

FIG. 3. Charge retention after programming at 10 V for 20 s, monitored by time-dependent transient relative capacitance (a) and flat-band voltage shift (b), respectively.

poor-quality oxide, in which fast states are generated and respond to high-frequency (1 MHz) signals.

In Fig. 3, the charge retention properties, characterized by both relative capacitance [Fig. 3(a)] and transient flat-band voltage shift [ΔV_{fb}, Fig. 3(b)], of the $TiSi_2/Si$ heteronanocrystal MOS memory are shown, where the retention curve of the Si dot device is also presented as comparison. The read voltages for capacitance are −5 V and −2.5 V for the $TiSi_2/Si$ heteronanocrystal MOS and Si nanocrystal MOS, respectively, which are within the corresponding memory windows. The relative capacitance is defined as $|C(t)-C_N|/|C_W-C_N|$, where $C(t)$, C_N, and C_W are the capacitance at time t, the capacitance of the neutral device and the capacitance right after the writing operation, respectively. ΔV_{fb} is obtained by comparing the C-V curves from a charged state and the quasi-neutral state. The retention measurements were performed immediately after programming the devices by applying a voltage of 10 V on the gate for 20 s. The decays of both the transient capacitance and ΔV_{fb} for the $TiSi_2/Si$ heteronanocrystal MOS device are slower than those of the Si dot device. It is evident that the ΔV_{fb} decay of both heterodot device and Si dot device are stepwise decline functions, each including two decay mechanisms with different decay time constant. The two time constants are 1.42 and 0.114/decade for the Si dot device (No. New23) and 0.849 and 0.0154/decade for $TiSi_2/Si$ heteronanocrystal device (No. 221), respectively. The faster decay procedures for both Si nanocrystal and $TiSi_2/Si$ heteronanocrystal devices in the earlier retention stage are believed to arise from poor-quality tunneling oxide, which induces leaky paths and shallow defect-related charge traps. Electrons trapped in those sites are easier to leak back to the substrate. The slower processes in the later retention stage for these two devices are due to the deeper levels in/on Si dots and the ground energy levels of the silicide dots that are much lower than the conduction-band edge of the substrate. It is noted that the decay constant in the later retention stage of the heterodot device is 7.5 times smaller than that of the Si dot device, indicating significantly improved charge retention ability of $TiSi_2/Si$ heteronanocrystal memory over Si nanocrystal memory.

It should be mentioned that the retention times of both the Si nanocrystal and $TiSi_2/Si$ heteronanocrystal MOS memories are quite short. This is primarily attributed to the poor quality of the tunneling oxide, which contains a large amount of defects and favors the leakage via trap-assisted tunneling. However, the device performance improvement by using $TiSi_2/Si$ heteronanocrystals to replace Si nanocrystals has been demonstrated with the same poor-quality tunneling oxide. With optimized thermal oxide, it is expected that better retention performance can be achieved for these devices.

In summary, $TiSi_2/Si$ heteronanocrystals were fabricated successfully by using the salicide technique on Si nanocrystals resting on silicon oxide films. The MOS capacitor containing these heteronanocrystals exhibits 7.5 times improved charge retention characteristics while also possesses a wider memory window as compared to the Si nanocrystal memory device. It is promising to use $TiSi_2/Si$ heteronanocrystals to replace Si nanocrystals for the next generation floating gate flash memory devices.

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