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Charge storage in a metal–oxide–semiconductor capacitor containing cobalt nanocrystals

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Abstract

Self-assembled cobalt (Co) nanocrystals on ultra-thin silicon dioxide layer were fabricated by in situ annealing Co ultrathin films deposited with Co effusion cell in a molecular-beam-epitaxy chamber. The resultant nanocrystals obtained at the optimized annealing temperature are around 3–4 nm in diameter with dot density of about 1×10^{12} cm^{-2}. The metal–oxide–semiconductor capacitors containing Co nanocrystals exhibit much longer retention times than a Si nanocrystal memory with the same tunneling oxide thickness. This study suggests that Co nanocrystal should be an excellent alternative to replace Si nanocrystal as floating gates for future nonvolatile flash-type memory application.
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1. Introduction

The employment of Si nanocrystals as discrete floating gates [1] is a promising way to limit the lateral charge communication in an electrically erasable programmable read-only memory (EEPROM), which in consequence provides a means for extending the scaling limit of flash memories. However, the long retention times observed in experiments for Si nanocrystal memories are believed to arise from the traps and defects inside or at the surface of nanocrystals [2]. These defects limit the application of Si nanocrystals for nonvolatile memory since they are very sensitive to annealing processes during device integration. Although the application of Ge nanocrystals as floating gate helps in principle the hole retention due to the valence band offset of Ge/Si system, the electron storage is degraded as compared with a Si nanocrystal memory [3]. Moreover, Ge atoms easily penetrate the tunneling oxide and degrade the device performance [4]. The effect of traps and defects can be depressed by using metal nanocrystals as floating gate [5,6]. Due to high density of states, metal nanocrystals not only rule out the effect of traps and defects, but also offer strong coupling between the nanocrystal and the substrate [5], which ensures high charge injection efficiency even at low operation voltages. Metal nanocrystals, including Au, Ag, Pt, W [5,6] and Ni [7] have been used as floating gates in nonvolatile memories. Co metal with work function of around 4.4 eV is another excellent material of choice for floating gate of a memory. However, little research on Co nanocrystals has been reported to date [8]. In this work, we experimentally demonstrate the memory effect of metal–oxide–semiconductor capacitor (MOSC) devices with Co nanocrystals of different densities embedded in

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SiO_2 and show their advantage over a Si nanocrystal memory.

2. Device fabrication and characterization

A chemically cleaned p-type 4-in. Si wafer with resistivity of about 10 Ω · cm was thermally oxidized in dry oxygen at 1000 °C for 4 min, which results in a thermal oxide with thickness of about 4–5 nm. This oxidized wafer was then transferred to a molecular-beam-epitaxy (MBE) chamber and a 1.5-nm-thick metal Co wetting layer was deposited at room temperature by using a Co effusion cell. The sample was subsequently annealed in situ in vacuum for 10 min with annealing temperature ranging from 500 °C to 800 °C, followed by a 15-nm-thick control oxide deposition in a low-pressure chemical-vapor-deposition (LPCVD) furnace. Finally, the 400-nm-thick aluminum electrodes were fabricated with the pattern size of 400 μm × 250 μm using lift-off process. The parameters of device fabrication are given in Table 1. The nanocrystals were characterized using both cross-sectional transmission electron microscope (TEM) and atomic force microscope (AFM). The memory characteristics were measured by high-frequency (1 MHz) capacitance–voltage (*C*–*V*), transient capacitance–time (*C*–*t*), and conductance–time (*G*–*t*) [9] techniques. In the *C*–*V* and *G*–*V* sweeping measurements, the flat-band voltage shift (ΔV_{fb}) is obtained from the shift of two branches of the *C*–*V* or *G*–*V* curves for the forward and backward sweepings, respectively. Therefore, in the data retention measurement, ΔV_{fb} is the shift of hysteresis curves between a programmed device and a neutral device, which can be derived by a modified constant-capacitance method [2].

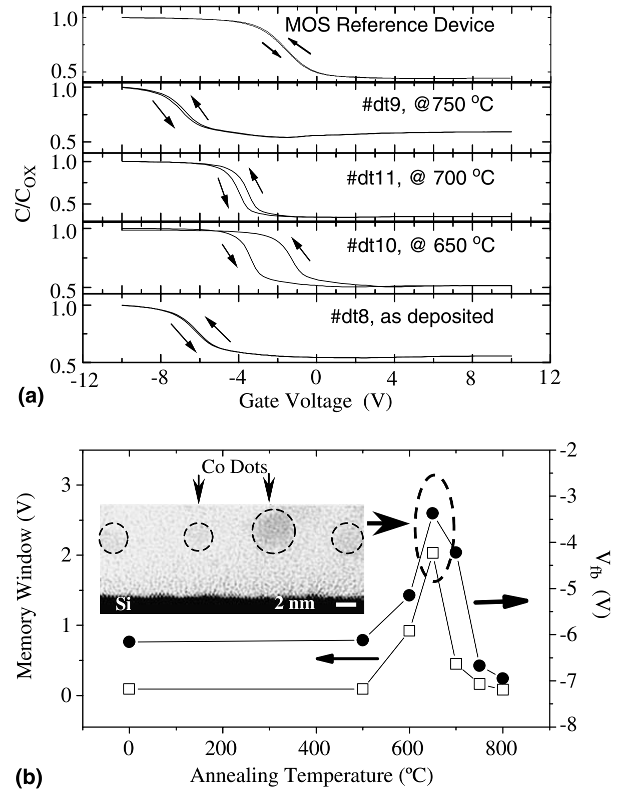

Fig. 1. (a) *C*–*V* characteristics, and (b) memory windows and the flat-band voltage in the forward-sweep *C*–*V* branch for samples in situ treated with different annealing temperatures in vacuum for 10 min. The inset in (b) is the cross-sectional TEM image of sample #dt10, which has the highest Co dot density of 1×10^{12} cm^2 as well as good electrical isolation between adjacent nanocrystals. The CV of a reference MOS capacitor without nanocrystals is also shown in (a) for comparison.

3. Results and discussion

The high-frequency *C*–*V* characteristics are shown in Fig. 1(a) for samples annealed at different temperatures with the annealing times all fixed at 10 min and a MOSC reference sample. The gate voltage swept from the inversion region to the accumulation region with a ramping speed of 0.2 V/s and then swept back. Flat-band voltages of all devices are of negative values as a result of aluminium electrode and possible fixed positive charge in the interface. All samples containing Co floating gates exhibit hysteresis loops while no hysteresis features can be found for a MOSC reference sample without Co nanocrystals, confirming that the memory effect originates from the presence of the Co embedded in the silicon oxide. A wider memory window (ΔV_{fb}) means a greater memory capacity [10]. One notices a very small (∼0.09 V) memory window for sample #dt8 which contains the *as-deposited* Co layer. The memory window increases slightly to 0.095 V when the annealing temperature increases to 500 °C. It reaches 2.1 V for sample #dt10, in which the Co layer was annealed at 650 °C. However, the memory window decreases between 0.45 V and 0.16 V as the annealing temperature increases between 700 °C and 750 °C, respectively. Fig. 1(b) summaries the memory window as a function of the annealing temperature. It should be noticed that as the memory window increases, the flat-band voltage (V_{fb}) on the forward-sweep branch of the *C*–*V* curve shifts towards positive voltage until the annealing temperature reaches 650 °C, when both the memory window and the flat-band voltage achieve their maximum. Beyond 600 °C, the memory window and the flat-band voltage decline again, as shown in Fig. 1(b).

The effect of annealing temperature on the memory window can be interpreted by the varied charge communication within the tunneling oxide plane as a result of the

Table 1
Parameters of device fabrication for Co nanocrystal memories and Si nanocrystal memory

Sample	Tunneling oxide thickness (nm)	Co layer thickness (nm)	Dot annealing temperature (°C)	Control oxide thickness (nm)
#dt8	4–5	1.5	As-deposited	15
#dt9	4–5	1.5	750	15
#dt10	4–5	1.5	650	15
#dt11	4–5	1.5	700	15
#16-1	4–5	Si dots	650	15

varied Co adatom diffusion ability at different annealing temperature. Generally the relaxation of the stress accommodation during the film deposition and the surface minimization are two main driving and limiting factors for the nanocrystal formation during the annealing [5,7]. Larger nanocrystals are formed at higher temperatures of 700 °C and 750 °C at the expense of decreased dot density [7], leading to smaller memory window of 0.45 V and 0.16 V, respectively [11]. For lower annealing temperatures (500 °C or less), the Co adatoms do not have sufficient energy to migrate so that the adjacent dots are very close or connect to each other. In other words, the floating gate is still an electrically continuous film. It is well known that the continuous floating gate possesses a worse retention due to the fact that even one conducting path in the tunneling oxide can drain out all charges in the floating gate. As annealing temperature goes too high, for example 750 °C, the reaction between metal and tunneling oxide might occur and degrade the tunneling oxide. This degradation increases the probability of faster tunneling through some conducting paths (weak points) significantly and results in a similar *C–V* behavior to the case of low annealing temperature (Fig. 1(a)). Only at suitable intermediate annealing temperature, such as 650 °C for #dt10, the resultant nanocrystals are of high density and fully discrete. The cross-sectional TEM image of #dt10 is shown in the inset of Fig. 1(b), where the Co nanocrystals with diameter of 3–4 nm can be clearly seen. The density of dots was estimated from a similar sample without control oxide to be 1×10^{12} cm^{-2} by AFM. The varied charge exchange ability also affects the efficiency of charge injection to the floating gate, namely the flat-band voltage, as exhibited in Fig. 1(b). Charge injection can occur easily through the conducting paths in tunneling oxide and fills the whole floating gate until the writing is saturated if the floating gate is continuous. Therefore, the fat-band voltage of these samples, such as #dt8, exhibit more negative values in the forward-sweep *C–V* branch. In the mean time, the concurrence of paths in tunneling oxide and continuous Co distribution degrades the memory characteristics, leading to narrower memory window, as shown in Fig. 1(b).

The charge retention characteristics, including the time-dependent transient conductance *G–t* and the flat-band voltage shift ΔV_{fb}–*t* are shown in Fig. 2(a) and (b), respectively for sample #dt10 (Co nanocrystal MOSC, annealed at 650 °C) at zero retention voltage after a programming operation at +10 V for 2 s. As a comparison, the results are also presented for a Si nanocrystal MOSC (sample #16–1) with the same tunneling oxide thickness. It is found that the conductance of Co MOSC exhibits a much lower level than that of the Si nanocrystal MOSC. This is probably due to the large amount of shallow traps in/on Si nanocrystals. These shallow traps have short trapping/detrapping times and thus can follow the high-frequency signals in the *C–V* measurements and result in greater AC conductance. Moreover, the decay of the conductance for Co nanocrystal MOSC #dt10 is also much slower than Si

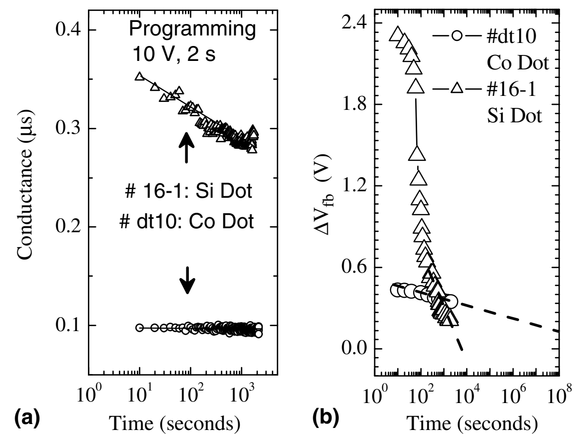

Fig. 2. (a) Time-dependent high-frequency (1 MHz) conductance, and (b) flat-band voltage shift evolution with time of holding the sample after programming at 10 V for 2 s. #dt10 and #16–1 are a Co nanocrystal MOS device and a Si nanocrystal MOS device, respectively.

nanocrystal MOSC #16–1, indicating a longer retention time for the Co nanocrystal capacitor, as can also be seen in Fig. 2(b). There are two noticeable differences between the retention curves for Si nanocrystal MOSC #16–1 and Co nanocrystal MOSC #dt10 in Fig. 2(b). First, ΔV_{fb} of #dt10 is smaller than that of #16–1 at the early stage of retention. Second, ΔV_{fb} of device #16–1 decays rapidly while that of device #dt10 decays slowly as time lapses.

The ΔV_{fb} difference at the early retention stage might be due to Coulomb blockade effect for the embedded nanocrystals. The size of Si nanocrystal in MOSC #16–1 is around 25 nm while that Co nanocrystals in MOSC #dt10 are only 3–4 nm. Therefore programming the Co nanocrystals is easier to be saturated by Coulomb repulsion from the charge already injected to the nanocrystals. In other words, the charge amount in each Co nanocrystal of #dt10 is much less than that in each Si nanocrystal of #16–1. Since the control oxide thickness is the same in both devices, the flat-band voltage shift in Co nanocrystal capacitor is smaller.

Based on the faster charge loss in sample #16–1, it is believed that the charge storage in a Si dot memory occurs via the defect-related shallow traps [2,12]. These traps are occupied by electrons injected by a positive voltage programming and emit electrons very fast. Therefore, despite its higher initial value, ΔV_{fb} of the Si dot MOSC (#16–1) decreases much faster than the Co dot device. Within 600 s it decreases from 2.3 V to 0.36 V. The decay curve does not follow a simple exponential decay law, indicating that there are traps with multiple levels in Si dot sample #16–1. On the contrary, thanks to the work function difference between Co and Si substrate, which aligns the Fermi level of Co almost with the midgap level of Si, the stored charges have to overcome the work function difference first before they can tunnel back to the substrate during retention. Therefore, a longer retention is achieved, as shown in Fig. 2(b). Due to the absence of band gap for metal Co, even though there exist interface/surface states on

metal Co dots, the high density of states may eliminate the influence of these states. This leads to a simple exponential decay during retention. If we define the retention time (τ) as the time when half of the stored charge is lost, one finds that τ is $\sim$83 s and $\sim 1.3 \times 10^6$ s for Si dot MOSC #16–1 and Co dot MOSC #dt10, respectively. The retention time improvement after using Co nanocrystal to replace Si nanocrystals as floating gate is about 4 orders of magnitude.

4. Conclusion

In summary, self-assembled Co nanocrystals on ultra-thin SiO_2 were grown using MBE. The temperature of in situ annealing plays an important role in nanocrystal formation and the device performance. The MOS capacitors containing Co nanocrystals possess much longer retention times than a Si nanocrystal counterpart as a result of work function difference between Co and Si substrate.

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