Fabrication of silicon quantum wires by anisotropic wet chemical etching and thermal oxidation

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Ultrafine silicon quantum wires with high-quality Si/SiO_2 heterointerfaces are successfully fabricated by utilizing anisotropic wet chemical etching and subsequent thermal oxidation. It is also found that the lateral dimensions of silicon quantum wires can be well controlled by selecting the temperature of the thermal oxidation process. The cross-sectional image from a scanning electron microscope shows silicon quantum wires of high quality with the linewidth down to 20 nm.

In subsequent years, Si-based integrated circuits will develop into nanoelectronics, that is, below submicron scale. As the basis of nanoelectronics, silicon quantum wires (SQWs) will play an important role in ultralarge scale integrations (ULSI) and high performance quantum effect devices.[1,2] Moreover, the band structure of artificially modulated silicon nanostructures is different from that of bulk silicon, which would make it possible to obtain new and novel optical properties and to apply them in silicon optoelectronic integrated devices.[3,4] During the last few years, much effort was invested in fabricating quantum wires of compound semiconductors.[5,6] In contrast, few attempts have been made to fabricate SQW, primarily due to the fact that it is quite difficult to make silicon single crystal nanostructures as compared to compound semiconductors either by deposition methods using chemical vapor deposition (CVD) and molecular beam epitaxy (MBE), or by selective etching. Recently, the interest in the fabrication and study of silicon nanostructures, as well as Si/SiGe quantum wires and dots, is increasing dramatically, e.g., Iwano *et al.* fabricated *p*-type silicon wires by selective implantation of focused Ga^+ ion beams,[7] Liu *et al.* used the oxidation method to thin silicon columns,[8] and the gas-source selective epitaxial growth technique has been used to generate SiGe quantum wires by Usami *et al.*[9] At the present stage, it is urgently necessary to develop advanced fabrication techniques to obtain SQWs of high quality.

In this report, we present briefly the fabrication of an array of the SQWs with a Si/SiO_2 heterointerface using anisotropic wet chemical etching and the subsequent thermal oxidation technique. Figure 1 shows a schematic of the SQWs fabricated in this work. An array of SQWs lies on the silicon substrate, where SQWs are embedded in a SiO_2 layer. Compared with the methods reported previously, the present one has many remarkable advantages, for example, the SQWs are produced with controllable lateral dimensions by selecting the temperature and time of thermal oxidation process; defect-free SQWs made of high-quality crystal can be achieved; electrons or holes are confined completely since the wide-band-gap SiO_2 acts as a high potential barrier. With the present fabrication process we ultimately produced the SQWs of high quality with the linewidth down to 20 nm; the observational result of the scanning electron microscope (SEM) is demonstrated.

In our fabrication steps of the SQWs, a (100) Si wafer is used as substrate. First, thermal oxidation technique is carried out to grow a 100 nm SiO_2 layer which acts as the mask for anisotropic wet chemical etching. Then, line-and-space patterns along the [011] direction with periods of 1.0–5.0 μm are formed by conventional lithography technique. Next, 350-nm-deep trenches are generated in the substrate by using reactive ion etching. After removing the photoresist, the substrate is dipped in ethylendiomine–pyrocatechol–water solution (EPW)[10] to form the silicon wires having upside down triangle cross sections on the top of the sawtooth structure with (111) facets. Subsequently, the nanostructure is thermally oxidized at high temperature (1000 °C) for some time in order to isolate the silicon wires from the substrate. Finally, the mid-temperature (below 850 °C) process of the thermal oxidation is used to thin the lateral dimensions of the SQWs. According to self-limiting oxidation effect,[11] when the oxidation temperatures are below 900 °C, i.e., in the self-limiting regime, the oxidation rate decreases with decreasing dimensions of silicon wires, and the limiting dimensions depend on the oxidation temperature.

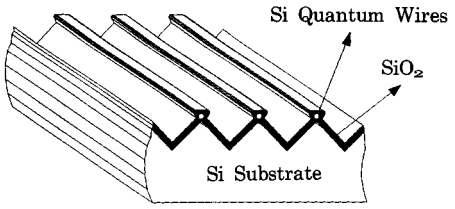

FIG. 1. Schematic of SQWs with the Si/SiO_2 heterointerfaces.

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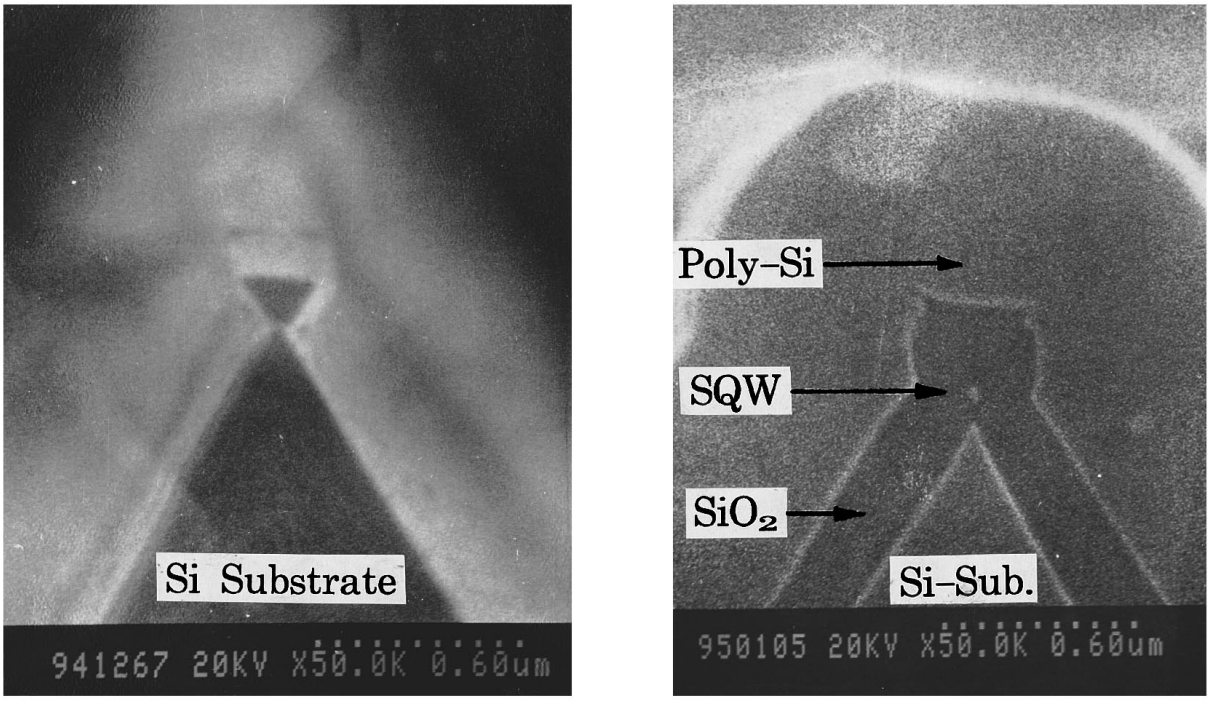

(a) (b)

FIG. 2. Cross-sectional image of SEM of (a) as-etched silicon wire with upside down triangle, (b) thinned SQW with a linewidth of ~20 nm.

Figure 2 shows scanning electron micrograph of SQWs. Prior to the thermal oxidation process, silicon wires with upside down triangles are prepared, as seen from Fig. 2(a). Figure 2(b) presents the cross-sectional image of SEM of a SQW embedded in the SiO_2 layer. In order to clearly observe it, we deposit a polycrystalline silicon mask on the SQWs by very low pressure chemical vapor deposition (VLP/CVD),[12] then cut the sample to appear in the cross section, and dip it in a buffered hydrogen fluoride solution to isolate the part of the SQWs from circumstances. As shown in Fig. 2(b), the linewidth of SQW is about 20 nm.

In conclusion, we have successfully fabricated the array of ultrafine SQWs with Si/SiO_2 heterointerfaces utilizing anisotropic wet chemical etching and subsequent thermal oxidation technique. It is found that the lateral dimensions of SQWs can be well controlled by the thermal oxidation process. Excellent results are evidenced by scanning electron microscope images. This attempt clearly shows the success of anisotropic wet chemical etching and thermal oxidation as a very valuable method for realizing SQWs of high quality.

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