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Simulation of a cobalt silicide/Si hetero-nanocrystal memory

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Abstract

A nanocrystal memory using $CoSi_2$/Si hetero-nanocrystals as floating gate was proposed. Numerical investigations on the writing, erasing and retention were performed. The hetero-structure provides an extra quantum well for the charge to achieve much longer retention time while maintains a writing/erasing speed similar to that of Si nanocrystal memory.
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1. Introduction

Si nanocrystals have been extensively investigated as floating gates in MOSFET memories [1–5]. Due to electrical isolation between nanocrystals, tunneling oxide can be very thin (~3 nm), leading to faster programming/erasing speed. However, the trade-off between long retention and fast programming/erasing for a traditional Si nanocrystal memory still remains as an obstacle for its practical application. To solve this issue, an interesting approach was proposed to use Ge/Si hetero-nanocrystals as floating gate in a p-channel MOSFET memory and the simulations showed that this structure could significantly prolong the retention time without decreasing the writing and erasing speeds [6]. In this paper, we propose a metallic silicide/Si hetero-nanocrystal memory. Metallic silicide material has a high density of states around Fermi level, which offers a strong coupling between the substrate and the nanocrystal [7]. In addition, owing to its metal-like nature, the valence band edge (E_v) and the conduction band edge (E_c) of some silicide materials, such as $TiSi_2$ [8] and $CoSi_2$ [9], are energetically located higher and lower, respectively, to the counterparts of the silicon. Therefore, a silicide/Si hetero-nanocrystal can be used for both p- and n-channel memories. Here we report simulation results on p-channel memory only to demonstrate the advantages of using $CoSi_2$/Si hetero-nanocrystals as the floating gate. The same procedures can be readily used to simulate electron storage in n-channel memory, which would reach the same conclusion of enhanced performance of hetero-nanocrystal memory over Si nanocrystal memory and is not shown here. It is worthwhile noting that $TiSi_2$/Si and $CoSi_2$/Si hetero-nanocrystals can be easily fabricated using self-aligned growth technique [8,9] on Si nanocrystals with a thorough compatibility to the existing Si VLSI process.

2. Device structure and simulation technique

Fig. 1 shows the schematic diagram and the band structure of a $CoSi_2$/Si hetero-nanocrystal memory. It should be noted that the valence band offset (ΔE_v) between $CoSi_2$ and Si is ~0.55 eV [10] and the band gap for $CoSi_2$ is zero. The charge communication between the control gate and the nanocrystal is neglected since the control oxide is assumed

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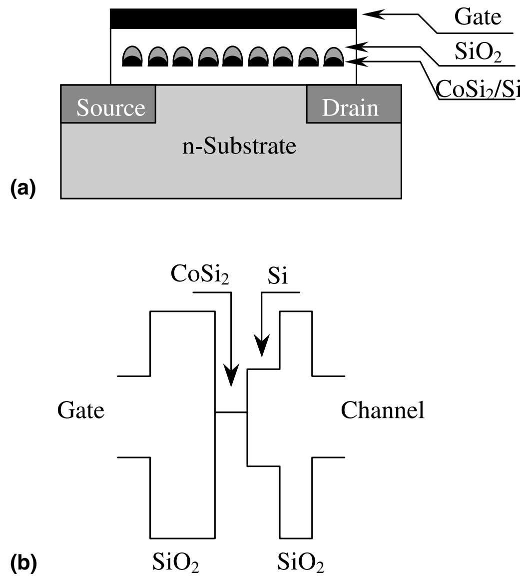

Fig. 1. The device structure (a) and the band diagram (b) of a $CoSi_2$/Si hetero-nanocrystal memory.

to be 5 nm, which is much thicker than tunneling oxide thickness assumed in our simulation with which direct-tunneling phenomenon normally takes over. For such a p-channel memory, the writing current, with a negative gate bias, consists of two components, namely the hole flux from substrate to the nanocrystals and electron flux from the nanocrystals to the substrate. Likewise, the erasing current is in general composed of electron flux from the substrate to the nanocrystals and hole flux from the nanocrystals to the substrate. The writing or erasing current can be calculated using [11]:

$$J = q\int_{E_{\text{shift}}\leqslant E} T(E)f(E)\rho(E)F_{1/2}(E)\,\mathrm{d}E \tag{1}$$

where $f(E)$ is the impact frequency, $\rho(E)$ the two-dimensional (2-D) density of states, $F_{1/2}(E)$ the Fermi–Dirac distribution function and $T(E)$ the tunneling probability, respectively. E_{shift} is the Si valence (for writing) or conduction band (for erasing) shift due to the quantum confinement effect from the small nanocrystal. The impact frequency reads [11]:

$$f(E) = 0.6\times\frac{2q}{(3\pi\hbar m_{\text{Si},\perp})^{1/3}}\left(\frac{\varepsilon_{\text{ox}}F_{\text{ox}}}{\varepsilon_{\text{Si}}}\right)^{2/3} \tag{2}$$

where $\hbar$, $m_{\text{Si},\perp}$, ε_{ox}, F_{ox}, and ε_{Si} are the reduced Planck's constant, the hole (or electron) effective mass perpendicular to the substrate, the dielectric constant of SiO_2, the surface electric field in SiO_2 layer, and the Si dielectric constant, respectively. The tunneling probability $T(E)$ is calculated using transfer matrix method [12].

The writing and erasing times are defined as the product of the elementary charge and the reciprocals of the tunneling currents in the writing and erasing processes, respectively. In the writing process, since the valence band edge of $CoSi_2$ is energetically higher than that of the Si substrate, the presence of $CoSi_2$ will not affect the hole current from the substrate to the floating gate. The hole erasure in a nanocrystal is mainly due to the electron current from the substrate to the nanocrystal. The hole current from the nanocrystal to substrate during erasing operation is orders of magnitude lower since the hole barrier (5.1 eV) is much higher than the electron barrier (3.1 eV). Therefore, the erasing has a speed similar to the writing process. The retention process is a two-step case: the hole, which is originally stored in the $CoSi_2$ region, first needs to be thermally activated to a quantum level of an energy equal or higher than the valence band edge of the substrate then has a probability to tunnel back to the substrate. The two-step case has a much lower probability than a single-step case for the carrier in a Si nanocrystal memory. In other words, it is expected that a $CoSi_2$/Si hetero-nanocrystal memory would have a much longer retention time than a Si nanocrystal memory. The retention time is defined as the time when $1/e$ charge remains [6], where e is the napierian base. Retention time then can be obtained by using a similar method to that used in [13] for a defective Si nanocrystal memory. In our case, we substitute the defect level with the effective quantum well (SiO_2/$CoSi_2$/Si) depth, namely [14]:

$$\tau = \frac{1}{\sum_{i=n}^{\infty}\exp\left(\frac{-(E_i-E_1)}{k_{\text{B}}T}\right)f(E_i)T(E_i)} \tag{3}$$

where E_i, E_1, K_{B} are the ith excited state and ground state (for holes) in the hetero-nanocrystal and Boltzmann's constant, respectively. The integer number 'n' is the quantum number from which the wave function spreads over both silicide and Si regions of the hetero-nanocrystal. The effective masses for the electron ($2m_0$) and hole ($4m_0$) in the $CoSi_2$ are taken from Ref. [10]. The eigen-energy levels are calculated with an improved shooting method [14] by simplifying a real quantum dot to a quantum box. As has been implemented in [13], the leakage current from the substrate to the nanocrystals is not considered during retention due to the fact that the electrostatic potential across the barrier layer is very small.

3. Results and discussion

Fig. 2 compares the writing and erasing characteristics of a $CoSi_2$/Si hetero-nanocrystal memory device with a Si nanocrystal memory device, where the Si dot height is fixed at 3 nm and the $CoSi_2$ dot height is 4 nm and 2 nm, respectively, with the base width all fixed at 3 nm. The tunneling oxide thickness is 1.9 nm. One observes that a much faster writing for the memory device with Si nanocrystals than the ones with $CoSi_2$/Si hetero-nanocrystals at gate voltage lower than 1.1 V only. This is attributed to the difference of electron current from the nanocrystals to the substrate at negative writing voltages. Since the conduction band edge of the $CoSi_2$ is lower than that of the Si nanocrystal, the electron emission rate from the Si nanocrystals is much higher than that from the $CoSi_2$/Si hetero-nanocrystals,

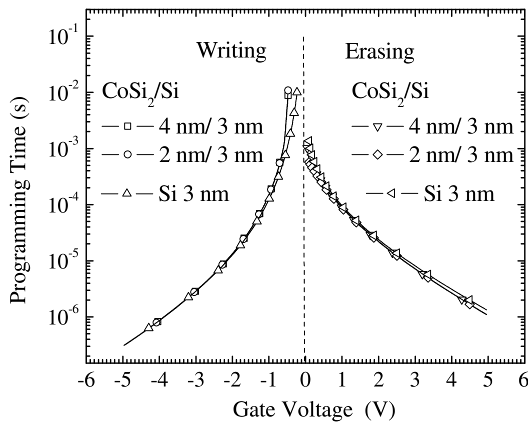

Fig. 2. The writing and erasing times with negative and positive voltage, respectively, as functions of the operation voltage for different nanocrystal sizes with the tunneling oxide thickness fixed at 1.9 nm for p-channel memory devices.

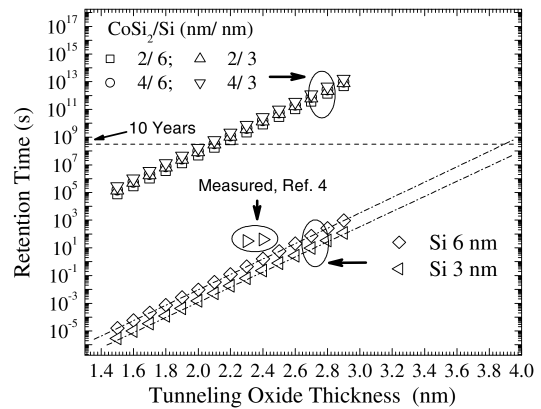

Fig. 3. The retention time as a function of the tunneling oxide thickness for a $CoSi_2$/Si hetero-nanocrystal memory and a Si nanocrystal memory as well. The presence of $CoSi_2$ on Si dot dramatically enhances the retention.

leading to a faster writing characteristics at lower voltage. Nevertheless, the difference in writing time tends to disappear as the writing voltage exceeds 2.0 V. It is clearly shown that both the 4-nm and the 2-nm $CoSi_2$ layers on the 3 nm Si dot produce the same writing characteristics. The writing time can achieve 0.3 μs at −5 V, which is very promising.

Since the electron tunneling current between the substrate and the hetero-nanocrystal is dominant, particularly at higher gate voltage, which is mainly because of the lower electron's barrier (3.1 eV) than the hole's barrier (4.5 eV), the erasing has a similar speed to that of the writing. Similar to the writing case, there are no obvious difference between a $CoSi_2$/Si hetero-nanocrystal memory and a Si nanocrystal memory in erasing process at higher erasing voltage. Nevertheless, the nanocrystal's electrostatic potential for the electrons is decreased as a result of to the presence of the holes, which are written during the writing, the erasing possesses a higher efficient compared with the writing case and erasing occurs at very small gate voltage. The erasing time reaches 1.1 μs at 5 V.

Though the presence of $CoSi_2$ on Si nanocrystal introduces no notable changes to either writing or erasing performance at higher voltages, it can significantly improve the retention time compared to a Si nanocrystal memory. Fig. 3 shows the retention characteristics as a function of the tunneling oxide thickness, where both the cases with defect-free Si nanocrystals and $CoSi_2$/Si hetero-nanocrystals are exhibited. Two Si nanocrystal sizes, namely 3 nm and 6 nm are investigated. To obtain a 10-year retention time for a Si nanocrystal memory, the tunneling oxide thickness should be as thick as 3.7 nm and 3.9 nm for the cases of 6 nm and 3 nm Si nanocrystals, respectively. With the same tunneling oxide thickness, the smaller (3 nm) Si dot leads to a shorter retention time due to the quantum confinement effect that raises the energy levels and increases the charge loss speed. Using such thick tunneling oxide, the writing and erasing of a Si nanocrystal memory would need high bias in the real device operation. This issue is easily solved by using $CoSi_2$/Si hetero-nanocrystals, as shown in Fig. 3, where it is found that even a 1.9 nm thick tunneling oxide achieves a 10-year retention time by using the $CoSi_2$/Si hetero-nanocrystals. However, using the same tunneling oxide thickness, a Si nanocrystal memory only shows a retention time of about 3 ms and 30 ms with Si dot size of 3 nm and 6 nm, respectively. The retention time improvement rate by adding $CoSi_2$ on Si nanocrystal can be as high as 10^9. Additionally, different from the case in a Si nanocrystal memory, the Si and $CoSi_2$ dot sizes of a $CoSi_2$/Si hetero-nanocrystal memory do not play important roles in affecting the retention time. The retention is only dominated by the tunneling oxide thickness, as is clearly illustrated in Fig. 3. This retention immunity from the dot size would greatly benefit the device fabrication tolerance and simplify the process. It is also noted that the retention improvement factor is based on the assumption that the Si nanocrystals are defect-free. Practical Si nanocrystals contain more or less defects, therefore charge traps, which improve the retention significantly [4], as also shown in Fig. 3. In our device, the deep quantum well with a band offset ~0.55 eV is artificially created by forming $CoSi_2$/Si structure, which leads to greater improvement, as clearly demonstrated in Fig. 3.

4. Conclusion

A $CoSi_2$/Si hetero-nanocrystal memory has been proposed and numerically simulated. It shows that for a $CoSi_2$/Si hetero-nanocrystal memory, the retention time of 10 years can be achieved with a 1.9 nm tunneling oxide. The sizes of $CoSi_2$ and Si nanocrystals do not influence the writing, erasing and retention characteristics for a $CoSi_2$/Si hetero-nanocrystal memory. With the same tunneling oxide thickness (1.9 nm) and Si nanocrystal size, the retention time for a Si nanocrystal memory is only several milliseconds. The erasing and writing times for the $CoSi_2$/Si hetero-nanocrystal memory reach 1.1 μs and 0.3 μs at ± 5 V, respectively. It concludes that the $CoSi_2$/Si hetero-

nanocrystal memory exhibits an obvious advantage over Si nanocrystal memory in data storage without affecting the writing/erasing performances.

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