Threshold voltage shift of heteronanocrystal floating gate flash memory

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Simulations of threshold voltage shift of a *p*-channel Ge/Si heteronanocrystal floating gate memory device were carried out using both a numerical two-dimensional Poisson–Boltzmann method and an equivalent circuit model. The results show that the presence of a Ge dot on top of a Si dot significantly prolongs the retention time of the device, indicated by the time decay behavior of the threshold voltage shift. Both methods lead to consistent results that an increase in the thickness of either the Si dot or Ge dot will result in a reduction of the threshold voltage shift. Additionally, the threshold voltage shift increases significantly as the heteronanocrystal density increases. Nevertheless, only a weak dependence of threshold voltage shift on the tunneling oxide thickness was found. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1847700]

I. INTRODUCTION

Nanocrystal floating gate memory has attracted increasing attention in the scaled flash memories for its faster speed, lower power consumption, and compatibility to traditional complementary metal-oxide-semiconductor processing.[1–3] In particular, silicon nanocrystal-based memory devices have been developed,[4–7] where electrons (or holes) tunneling into or out of the nanocrystals shift the device threshold voltage. The primary advantage of this memory structure is the low operation voltage due to the employment of an ultrathin tunneling oxide. However, there is a trade-off between a high programming speed and a long retention time. Generally a higher programming speed requires a thinner tunneling oxide, but incurs the penalty of leading to a shorter retention time. In order to overcome this issue, a metal-oxide-semiconductor-field-effect-transistor (MOSFET) memory storage cell has been proposed using Ge/Si heteronanocrystal in place of the Si nanocrystals.[8] Owing to the band offset at the interface of Ge/Si heteronanocrystal, a *p*-channel flash memory using heteronanocrystals as the floating gate can have a longer retention time while the programming speed is only slightly changed.[9] This phenomenon is also addressed by the time decay of the threshold voltage shift in this paper. As one of the most important parameters for flash memory, the threshold voltage shift (ΔV_{th}) can be an index of the memory state by measuring the source-drain current when a control gate bias is applied within the memory window.[10] Although there have been many papers, both theoretical[11,12] and experimental,[13,14] on ΔV_{th} of nanocrystal-based flash memories, a systematic investigation of the ΔV_{th} of heteronanocrystals-based flash memory is still lacking. In this work, the threshold voltage shift ΔV_{th} is investigated with a numerical method and an equivalent circuit model. The numerical approach offers a relatively accurate solution, though it is computationally time consuming. Conversely, the equivalent circuit model presents a possibility to estimate the dependence of ΔV_{th} on variable parameters from a global view and is physically clearer and easier to be realized. In the present work, the dependences of ΔV_{th} on nanocrystal size, nanocrystal density, and tunneling oxide thickness are studied for *p*-channel Ge/Si heteronanocrystal-based flash memory, using both the numerical method and the equivalent circuit method, showing that these two methods result in a good agreement with each other.

II. DEVICE STRUCTURE AND MODEL

Figure 1(a) shows the schematic cross section of a *p*-channel Ge/Si heteronanocrystal-based flash memory. Ge/Si heteronanocrystals are embedded in the oxide layer between the control gate and the *n*-type Si substrate. Assuming a regular dot distribution, a periodic boundary condition along the channel is used. Figure 1(b) is the simulation cell used in our numerical investigation, which is a symmetric subcell of an actual memory device.

The electrical potential ϕ (with respect to the substrate potential) satisfies the Poisson–Boltzmann's equation in Eq. (1),

$$\nabla \cdot (\varepsilon \nabla \phi) = -q(p - n + D), \tag{1}$$

where q is the elementary electron charge, ε is the material permittivity, n and p are the mobile electron and hole densities, respectively, and D is the concentration of ionized impurities (*n*-type doping). For nondegenerate semiconductors

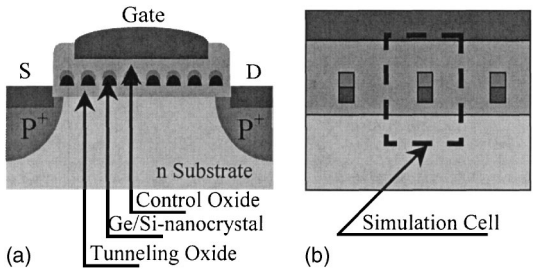

FIG. 1. (a) The structure diagram of the heteronanocrystal floating gate flash memory. (b) Simulation cell with a periodic boundary condition in the lateral direction and the ohmic contact for the electrical contacts.

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with parabolic band structures in equilibrium, densities n and p can be related to ϕ by Boltzmann's statistics:

$$n = n_0 e^{q\phi/kT}, \tag{2}$$

$$p = p_0 e^{-q\phi/kT}, \tag{3}$$

where n_0 and p_0 are the equilibrium concentration of electrons and holes deep in the substrate, respectively. In a two-dimensional frame, the finite difference iterative format reads

$$\phi_{i,j} = \frac{(\varepsilon_{i+1,j}\phi_{i+1,j} + \varepsilon_{i,j}\phi_{i-1,j})\Delta y^2 + (\varepsilon_{i,j+1}\phi_{i,j+1} + \varepsilon_{i,j}\phi_{i,j-1})\Delta x^2 + \rho\Delta x^2\Delta y^2}{(\varepsilon_{i,j} + \varepsilon_{i+1,j})\Delta y^2 + (\varepsilon_{i,j} + \varepsilon_{i,j+1})\Delta x^2}, \tag{4}$$

where Δx and Δy are the iteration steps along and perpendicular to the channel, respectively. One finds that the dielectric constant is involved in the iteration. This treatment greatly benefits the simulation since the special consideration at interfaces between different materials is naturally canceled out. The Jacobi relaxation method is applied to solve the differential equation. An initial guess is made for the node voltages. The iteration is applied alternately, updating the node values as well as the electron and hole densities, until the potential at each node converges to a stable solution. In all simulations, the thickness sum of the Si dot, Ge dot, and the control oxide is kept constant at 10 nm. Different from the method used in Ref. 12, where the drain current is used to determine the threshold, in this work the threshold voltage is defined as the gate voltage at which the minimum hole density (along the channel direction) at the Si/SiO_2 interface reaches the electron density iin the n-type substrate. This definition makes the simulation easier since it only use a metal-oxide-semiconductor (MOS) structure instead of a MOSFET in Ref. 12. For simplicity, while not being far from reality, the control gate contact and substrate contact were treated as ideal ohmic contacts.

Although the above numerical method provides an accurate solution, a simple circuit model offers a global view of the device behavior with suitable approximations made while being easy to understand. Such an equivalent device model uses several parallel-plate capacitors, as shown in Fig. 2. ΔV_{th} can be evaluated using the following expression:

$$\Delta V_{\text{th}} = \frac{\Delta Q_{\text{eff}}}{C_{\text{total}}}, \tag{5}$$

where C_{total} and Q_{eff} are defined in Eqs. (6) and (7),[15] respectively:

$$\frac{1}{C_{\text{total}}} = \frac{1}{C_{21}} + \frac{1}{C_{22}} + \frac{1}{C_{23}} + \frac{1}{C_{24}}, \tag{6}$$

$$Q_{\text{eff}} = \frac{\varepsilon_{\text{ox}}}{d}\int_0^d \frac{x\rho(x)}{\varepsilon(x)}dx. \tag{7}$$

Here, C_1 is the mutual capacitance between the control gate and the channel area not covered by the nanocrystals. C_{21}, C_{22}, C_{23}, and C_{24} are the mutual capacitances between the control gate and the Ge dot, the self-capacitances of the Ge dot and Si dot, and the mutual capacitance between the Si dot and the channel, respectively. Q_{eff} stands for the equivalent charge at the Si/SiO_2 interface induced by the charge in the nanocrystal. The integral begins from the interface of the control gate/control oxide to the interface of the tunneling oxide/Si substrate. Different permittivities are involved in the equation so that the effect of different materials can be included. Notice that the concept of $Q_{\text{eff}}$for the nanocrystal memory device is used instead of the real charge in the nanocrystal for the calculation of ΔV_{th}. This is very similar to the case of a MOSFET with a fixed charge in the oxide insulator[15] where the location of the fixed charge in the oxide will significantly affect the threshold voltage.

III. RESULTS AND DISCUSSION

The hole density near the Si/SiO_2 interface as a function of the applied gate voltage is shown in Fig. 3, where tunneling oxides of 2.07 nm, Si dot of 2 nm, Ge dot of 3 nm, and control oxide of 5 nm are assumed. The two curves in Fig. 3 represent the cases of the device being charged ($N=1$) and not charged ($N=0$). One observes a shift of about -0.65 V for the charged device with respect to the device not charged.

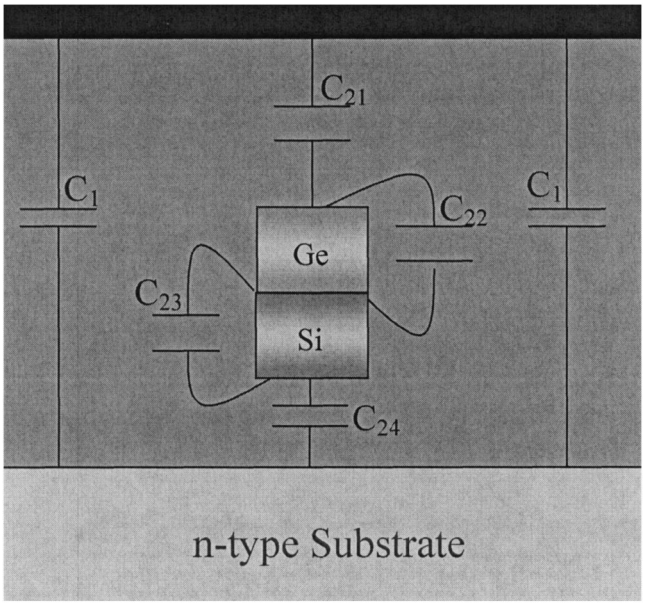

FIG. 2. The diagram of the equivalent circuit model for the flash memory. The capacitors in this model are ideal parallel-plate capacitors.

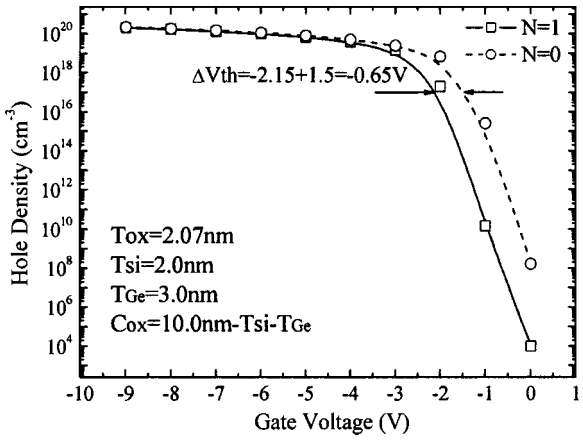

FIG. 3. The hole density on Si/SiO_2 interface as a function of gate voltage. The threshold voltage is defined as the voltage where the interfacial hole concentration equals to the electron concentration in the *n*-type substrate. T_{ox}, T_{Si}, T_{Ge}, and C_{ox} represent the thicknesses of the tunneling oxide, Si dot, Ge dot, and control oxide, respectively. N indicates the charge status of the device ($N=1$ for the charged status and $N=0$ for the uncharged status).

The retention time of flash memory sensitively depends on the tunneling oxide thickness and the presence of the Ge dot on top of the Si dot.[9] The Ge/Si heteronanocrystals can significantly prolong the retention time. Our numerical calculation, which will be published elsewhere, shows that for the case using only Si (2 nm) nanocrystal as the floating gate, a 2.07-nm-thick tunneling oxide is needed to achieve the ten-year requirement of retention time. However, if the Ge/Si (3 nm/2 nm) heteronanocrystal is present, the tunneling oxide can be as thin as 1.36 nm in order to obtain the same retention time. In Fig. 4, ΔV_{th} is calculated at a different time of charge storage for the cases with and without the Ge dot on top of the Si nanocrystal, respectively. It is found that if only Si nanocrystals are present as the floating gate and the thickness of the tunneling oxide is 2.07 nm (curve 3), ΔV_{th} immediately after the charge injection can be as high as -1.8 V. ΔV_{th} declines more rapidly than the other two curves with Ge/Si heteronanocrystals, where the tunneling oxides are 2.07 nm (curve 1) and 1.36 nm (curve 2), respectively. Regarding the case where the tunneling oxide is 2.07 nm and Ge/Si heteronanocrystals are used, the reduction of ΔV_{th} is almost zero for ten years of retention time.

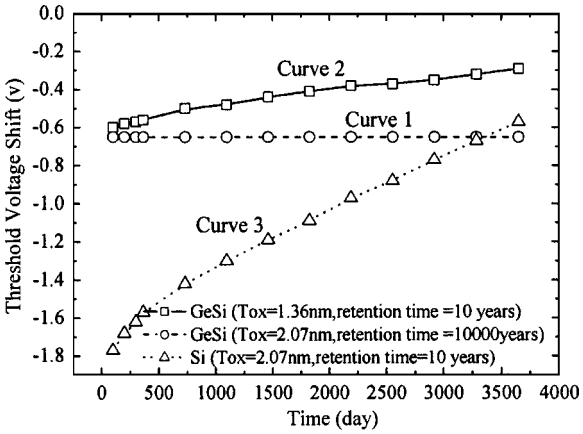

FIG. 4. The threshold voltage shift as a function of storage time for three cases.

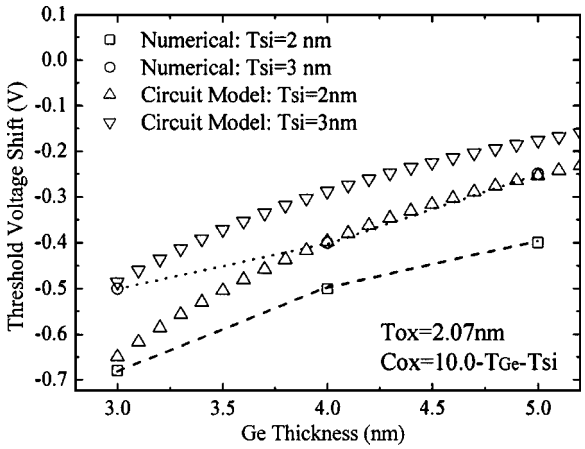

FIG. 5. The threshold voltage shift as a function of the Ge dot thickness. Two cases of different Si dot sizes are presented, respectively. The increase of either the Si or Ge dot size will decrease the threshold voltage shift. The data from the equivalent circuit model with a phenomenological effective screen length $0.3L$ are also shown, where L is the interdot distance.

The dependence of ΔV_{th} on the Ge dot thickness is shown in Fig. 5 (labeled as "numerical") where the tunneling oxide is 2.07 nm and the lateral simulation cell size (L) is 14 nm which corresponds to a dot density of 5×10^{12} cm^{-2}. Two thicknesses of the Si dot (2 and 3 nm, respectively) are investigated. It is shown that ΔV_{th} decreases as the Ge dot thickness increases. A reduction in ΔV_{th} of 0.25 V can be found when the Ge dot thickness varies from 3 to 5 nm for a fixed Si dot size. It also shows that a thinner Si dot leads to larger $|\Delta V_{th}|$. A 1-nm Si dot thickness difference can introduce a ΔV_{th} difference of about -0.2 V.

In Fig. 6 the dependence of ΔV_{th} on the tunneling oxide thickness is shown (labeled as numerical). The Si and Ge dots are 2 and 3 nm, respectively. When the tunneling oxide thickness varies from 3 to 5 nm, the change of ΔV_{th} is about 0.05 V. The dependence of ΔV_{th} on nanocrystal dot density is illustrated in Fig. 7 where $|\Delta V_{th}|$ increases from 0.38 to 0.68 V as the dot density changes from 2.7×10^{11} to 6×10^{11} cm^{-2}, corresponding to the dot-to-dot distance changing from 19 to 13 nm.

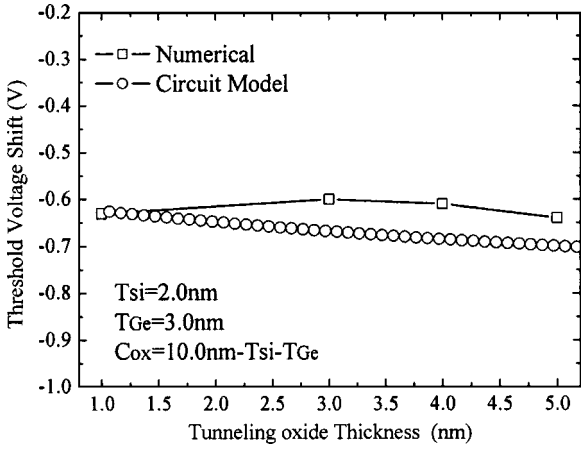

FIG. 6. The threshold voltage shift as a function of the tunneling oxide thickness. Only a weak dependence of the threshold voltage shift on the tunneling oxide thickness can be found. The data from the equivalent circuit model with a phenomenological effective screen length $0.3L$ are also shown.

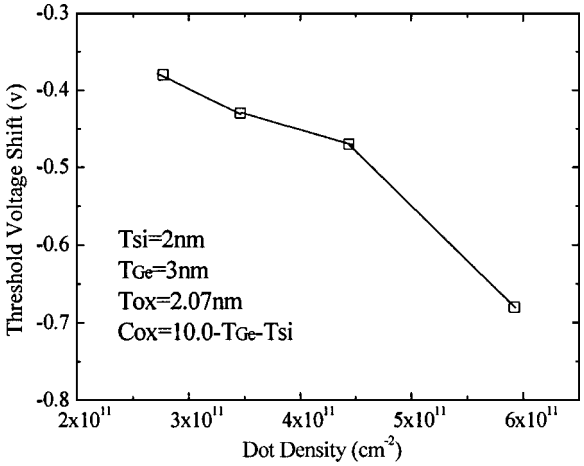

FIG. 7. The threshold voltage shift changes with the dot density. Higher dot density leads to larger threshold voltage shift.

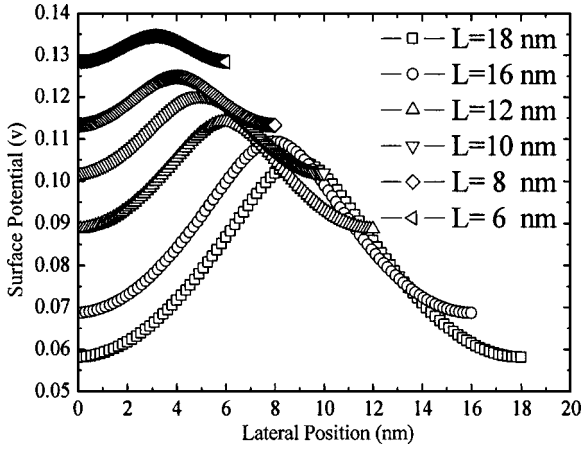

FIG. 8. The potential distribution along the channel with the gate voltage equaling 0 V for different interdot distances (L). Only when L is comparable to the dot size, the effective capacitor area for threshold voltage shift estimation can be equal to the whole device area.

In order to clearly understand the behavior of ΔV_{th} obtained from numerical results based on Poisson's equation, the equivalent circuit model is employed as introduced previously. For simplicity, the ideal parallel-plate capacitor model is used for all the capacitors introduced in this equivalent circuit model. The capacitance of C_{l} is not taken into account since it is the most difficult part to be inverted to decide the threshold voltage. For both the Si and Ge nanocrystals, one can simply use the parallel-plate model with the plate areas equal to the dot cross sections. However, the area that is screened by the charge stored in the nanocrystal, namely, the capacitor area for C_{24}, is not straightforward although it has been discussed in Refs. 13 and 14, where the whole channel area is used as the screen area. The determinations therein are based on the comparison between their estimation and the experimental data. As suggested above [Eqs. (5) and (7)], the equivalent charge instead of just the real trapped charge will be used for the ΔV_{th} estimation. The equivalent charge is generally one order of magnitude lower than the actual charge trapped in the nanocrystal. Therefore, a corresponding larger capacitor area is reasonably necessary in Refs. 13 and 14 for fitting a given ΔV_{th} measured experimentally. However, our numerical calculation has shown that this approximation using the whole channel area is only valid when the interdot distance is so small that the potential distribution over the whole channel is much more uniform than the case of a larger interdot distance. Figure 8 depicts the calculated surface potential along the channel (source-drain direction) for several interdot distances. For the case of larger dot-to-dot distances, the potential distribution is quite uneven thus the whole channel area cannot be accepted as the capacitor area in our calculation when the equivalent charge is implemented. In addition, the fact that the potential not only distributes under the nanocrystal but also covers other parts of the channel indicates that the employment of only nanocrystal area is not suitable. Therefore, it is reasonable to use an effective area whose value falls between the whole device area and the area covered by the nanocrystal. However, the derivation of an analytic value of the effective area is very difficult and we have only used a phenomenological fitting here. In Fig. 9, ΔV_{th} as a function of dot density is plotted using the effective screening length of 0.3 times interdot distance. For comparison, the results with the whole device length and the nanocrystal size only are shown as well, where the data obtained from the numerical solution of Poisson's equation are also plotted as a reference. It is obvious that the approximations using either the whole device area or using the nanocrystal size are not consistent with the data from Poisson's equation, while the approximation using 0.3 times the interdot distance matches the data from the numerical calculations, particularly for the case of smaller dot densities.

The dependence of ΔV_{th} on the thicknesses of the Ge dot, Si dot, and the tunneling oxide are shown in Figs. 5 and 6, respectively, using the equivalent circuit model. One can see an encouraging agreement between this approximation and the numerical method.

Based on the circuit model, the behavior of ΔV_{th} can be interpreted. Since the charge is only in the Ge dot, Eq. (7) can be simplified as,

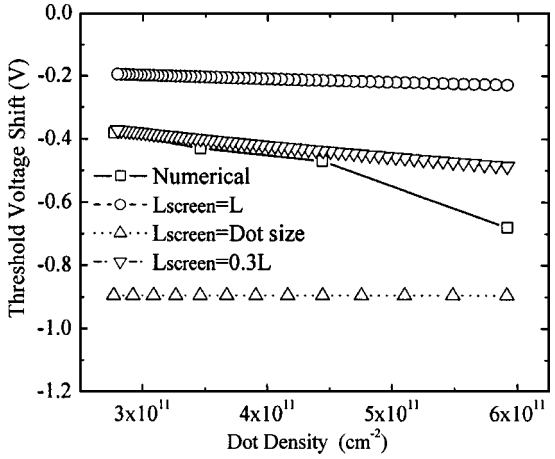

FIG. 9. A comparison between the numerical method and the equivalent circuit model. The phenomenological effective screen lengths (L_{screen}) are chosen as L 0.3L, and the Ge dot size in the equivalent circuit model, respectively. L is the interdot distance. Only the result based on the screen length of 0.3L matches the numerical data.

$$Q_{\text{eff}} = \frac{\varepsilon_{\text{ox}} q}{\varepsilon_{\text{Ge}}} \frac{10\ \text{nm} - T_{\text{Si}} - 0.5T_{\text{Ge}}}{10\ \text{nm} + T_{\text{ox}}},$$

where $T_{\text{Si}}+T_{\text{Ge}}+C_{\text{Ox}}=10$ nm is used with $T_{\text{Si}}, T_{\text{Ge}}, C_{\text{Ox}}$ the thickness of the Si dot, Ge dot, and control oxide, respectively. It is clear that an increase of either the Si dot or Ge dot thickness leads to a reduction in Q_{eff}. Meanwhile, the increase of either the Si dot or Ge dot thickness results in an increase in total capacitance, C_{total}. The net effect is that greater Ge or Si nanocrystal thickness corresponds to a smaller ΔV_{th} since $\Delta V_{\text{th}}=\Delta Q_{\text{eff}}/C_{\text{total}}$. In addition, as the tunneling oxide gets thicker, both C_{total} and Q_{eff} tend to get smaller. Therefore, ΔV_{th} as their quotient exhibits a weaker dependence on the tunneling oxide thickness.

IV. SUMMARY

The threshold voltage shift characteristics of a Ge/Si heteronanocrystal-based flash memory was investigated with both a numerical method and a simple circuit model. The calculations show that a larger shift in the threshold voltage can be achieved by decreasing the thickness of the Ge or Si nanocrystal. The shift increases with the dot density. However, the variation of the tunneling oxide thickness only slightly affects the threshold voltage shift. Both the rigorous numerical method and the simple circuit model approximations of the threshold voltage shift exhibit a good agreement with each other.

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