Effective compliant substrate for low-dislocation relaxed SiGe growth

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An effective compliant substrate was fabricated for the growth of high-quality relaxed SiGe templates, by synthesizing a 20% B_2O_3 concentration borosilicate glass (BSG) in the silicon on insulator wafers. Substrates with 5%, 10%, and 20% B_2O_3 were used for 150 nm $Si_{0.75}Ge_{0.25}$ epitaxy. Double-axis x-ray diffraction measurements determined the relaxation and composition of the $Si_{1-x}Ge_x$ layers. Cross-sectional transmission electron microscopy was used to observe the lattice of the SiGe epilayer and the Si substrate, dislocation density, and distribution. Raman spectroscopy was combined with step etch to study the samples. The strain sharing effect of the 20% BSG substrate was demonstrated. Thus, we concluded that this compliant substrate is a highly promising candidate for the growth of low-dislocation relaxed SiGe layers. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1351520]

In recent years, there has been considerable interest in relaxed SiGe buffer layers, which are used as ''virtual substrates'' for the growth of high electron mobility transistor, metal–oxide–semiconductor field effect transistor and the integration of III–V devices on Si.[1–3] However, the large lattice mismatch (~4.17%) between Si and Ge results in a high density of dislocations in SiGe buffer layers with high Ge content. Moreover, threading dislocations propagate through the SiGe buffer layer into the active layers and deteriorate the device performance.[4] To date, several strategies such as a graded composition growth[5] and using a low temperature buffer layer[6] have been explored to prepare relaxed SiGe layers minimizing the threading dislocation density.

The concept of compliant substrate was proposed by Lo in 1991[7] and was later realized experimentally by Powell *et al.* in 1994.[8] The ideal compliant substrate would be a freestanding thin substrate, which could elastically accommodate the misfit strain and absorb threading dislocations. In practice, however, a thin membrane acting as a substrate is prohibitive. Currently, there are several approaches to fabricate a compliant substrate by wafer bonding.[9,10] The thin silicon on insulator (SOI) substrates have been used as compliant substrate for GaN and SiGe epitaxy.[11,12] In the case of SiGe, the SiO_2 is expected to be rigid at the growth temperature range (typically between 450 and 700 °C). As a result, conventional SOI is not an effective compliant substrate and the relaxed SiGe layers grown on these kinds of substrates exhibited a large number of dislocations.[11] Therefore, to achieve an effective compliant substrate, it is necessary to realize that the SOI could deform at low growth temperature. It is well known that the addition of B_2O_3 in SiO_2 [borosilicate glass (BSG)] decreases the viscosity of the SiO_2.[13] For example, to have a 15 Poise viscosity in SiO_2, which is roughly the critical viscosity for the strain to transfer from the SiGe epilayer to the thin Si layer,[14] the temperature is 1100 °C. However, for 20% BSG, the temperature drops to 500 °C. In this work, the substrates with different concentrations of B_2O_3 in the SiO_2 layer of SOI wafers were fabricated and referred to as BSG substrates.[15]

The SOI substrates used in this work were bonding and etch back SOI (BESOI) wafers produced by Sibond, Inc. The fabrication process of our BSG substrates was as follows: BESOI wafers with a 60 nm Si layer and a 400 nm buried SiO_2 were implanted with boron and oxygen. The implant dosage and energy were selected according to the stoichiometrical ratio of B_2O_3 and the target concentration by weight.[16] After implantation, a two-step annealing process was performed to form the single crystal Si layer and the BSG layer. Solid phase epitaxy was performed at 500 °C for 2 h in nitrogen ambient. The wafers were subsequently annealed at 900 °C for 5 h in nitrogen ambient to form the borosilicate glass as well as minimize implantation damage. The top Si layer was thinned down to about 20 nm by thermal oxidation and HF dip. The surface morphology was analyzed by atomic force microscopy and found suitable for molecular beam epitaxy with the root mean squared roughness measured as 0.3 nm. The substrates were cleaned and immediately loaded into a Perkin–Elmer molecular beam epitaxy system.

BSG substrates with three weight ratios, 5%, 10%, and 20% B_2O_3, were used for SiGe epitaxy. For comparison, a SOI and a planar Si substrate were loaded simultaneously. The epitaxy sequence consisted of a 10 nm Si buffer layer, a 150 nm $Si_{0.75}Ge_{0.25}$ layer an 500 °C. The nominal deposition rates of Si and Ge were 1.2 and 0.4 Å/s, respectively. The sample grown on the 5% BSG substrate was named as 5% BSG sample in this letter, and it was the same way for other samples.

The double-axis x-ray diffraction (DAXRD) results of symmetric (004) and asymmetric (113) scan for the as-grown

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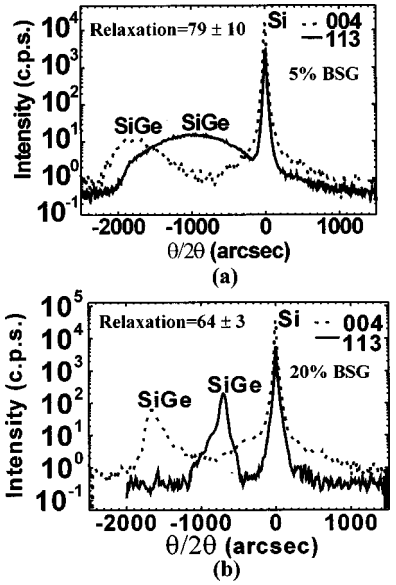

FIG. 1. Symmetric (004) and asymmetric (113) DAXRD measurements for (a) the as-grown 5% BSG sample and (b) the as-grown 20% BSG sample. The structure of the sample is 150 nm $Si_{0.75}Ge_{0.25}$/10 nm Si/20 nm Si/BSG.

and annealed 5% and 20% BSG samples are shown in Fig. 1, illustrating the relaxations of the SiGe layer. For the 5% BSG sample, due to the presence of misfit dislocations at the SiGe/Si interface, the SiGe peaks are broad as a result of mosaic structures. For the 20% BSG sample, the much narrower SiGe peaks indicate a much lower density of misfit dislocations. This would be expected if the thin silicon layer had become strained during growth.

The quality of the SiGe layers was compared by cross-sectional transmission electron microscope (XTEM) measurement using Philips CM200 FEG microscope. The images are shown in Figs. 2 and 3 and all of them are bright field cross-sectional [110] images. In Fig. 2(a), from careful measurement of the interatomic spacing, it is found that for the as-grown 5% BSG sample there is a lattice mismatch between the epilayer and the Si layer. A misfit dislocation and stacking fault can be observed in the SiGe/Si interface region

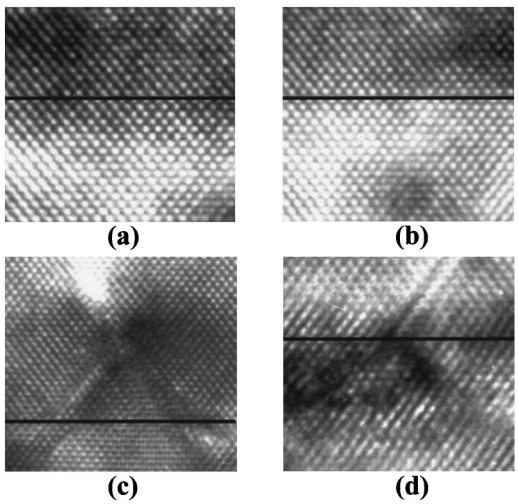

FIG. 2. High resolution transmission electron microscopy image of (a) the as-grown 5% BSG sample, (b) the 5% BSG sample annealed at 850 °C for 30 min in nitrogen ambient, (c) the as-grown 20% BSG sample, and (d) the 20% BSG sample annealed at 850 °C for 30 min in nitrogen ambient.

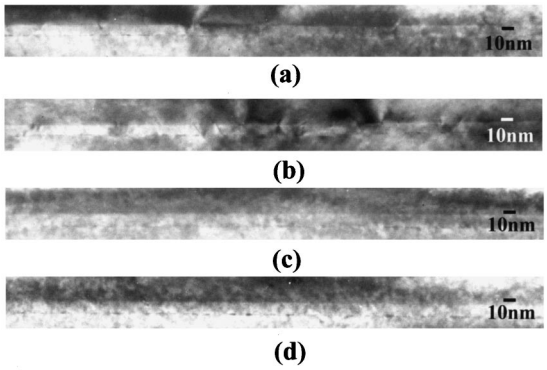

FIG. 3. XTEM image of (a) the as-grown 5% BSG sample, (b) the 5% BSG sample annealed at 850 °C for 30 min in nitrogen ambient, (c) the as-grown 20% BSG sample, and (d) the 20% BSG sample annealed at 850 °C for 30 min in nitrogen ambient.

too. In Fig. 2(b), it is found that after annealing the mismatch becomes larger than that of the as-grown sample, which implies that the SiGe layer relaxes more after annealing. For the as-grown 20% BSG sample shown in Fig. 2(c), every {100} double layer of the Si substrate continues into the SiGe layer, which indicates that the SiGe layer makes a coherent interface with the Si layer. Therefore, it appears that the Si substrate becomes tensily strained to match the SiGe layer. After annealing, as shown in Fig. 2(d), stacking faults are observed in the Si layer and the strained Si layer relax partially after annealing and dislocations form in it.

Densities of misfit dislocations were estimated from XTEM images with different magnifications. The largest observation range is about 5 μm. For the as-grown 5% BSG sample, as shown in Fig. 2(a), the diffuse contrast arises from the misfit dislocations and corresponding stacking faults are clearly observed in the SiGe/Si interface. The density of misfit dislocation was estimated to be 2×10^5 cm^{-1}. After annealing at 850 °C for 30 min, the density of misfit dislocations at the SiGe/Si interface increased to about 4×10^5 cm^{-1}, as shown in Fig. 2(b). For the 20% BSG sample, as shown in Fig. 2(c), no misfit dislocations are observed at the interface of the SiGe layer and Si layer in all images, suggesting that the density is below 2×10^3 cm^{-1} (the limit of detection). After annealing at 850 °C for 30 min, a threading dislocation is observed to propagate downwards into the Si buffer layer, as shown in Fig. 2(d). The density of misfit dislocation at the SiGe/Si interface increased to about 1×10^4 cm^{-1}.

The plastic strain relief δ is related to the misfit dislocation with density ρ_{md} by $\delta=b_{eff}\times\rho_{md}$, where b_{eff} is the effective Burger's vector, the component of the Burger's vector responsible for misfit strain relief. For 60° dislocation in SiGe, b_{eff} is $a_{SiGe}/2\sqrt{2}$. For fully relaxed $Si_{0.75}Ge_{0.25}$ on Si substrate, $\delta=1.04$. Then if the strain is completely released by plastic relaxation, i.e., due to the formation of misfit dislocations, from the above relation, we have $\rho_{md0}=5.36\times10^5$ cm^{-1}, where the subscript ''0'' indicates full relaxation. For partially relaxed $Si_{0.75}Ge_{0.25}$ with R% relaxation, $\rho_{md}=\rho_{md0}\times R\%$.

For the 5% samples, the measured misfit dislocation densities are a little lower than the calculated values. The reason is that the threading dislocations release part of the

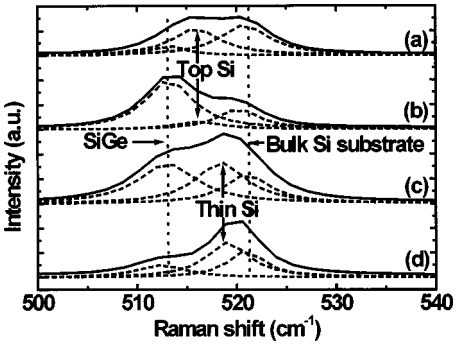

FIG. 4. Raman spectra from the as-grown 20% BSG sample: (a) without etching, and (b), (c), and (d) after etching steps. The dash curves are the fitted peaks using iterated Lorentzian fitting to the Raman spectrum. The letters with arrows in the figure indicate that the peak is the Si–Si mode of that layer. The SiGe means the SiGe layer. The top Si means the 5 nm Si layer on the top of the SiGe layer. The thin Si means the thin Si substrate beneath the SiGe layer. The bulk Si substrate means the bulk Si substrate beneath the SiO_2 layer of the SOI.

mismatch. In the XTEM images, stacking fault contrast decorates the region of the SiGe/Si interface. Threading dislocations propagate downwards into the Si layer, as well as upwards into the SiGe layer. The measured misfit dislocation densities for the 20% sample are much lower than the calculated values and no threading dislocation is observed in the SiGe layer and the Si layer. The reason for the fewer misfit dislocations is that the {100} lattice of the thin Si substrate expands to become strained to match that of the SiGe layer.

To confirm the strain in the thin Si substrate below the SiGe layer, Raman spectroscopy combined with step etch was used to further characterize the strain of the samples. Raman spectra were taken with a microscope entrance, giving a 0.7 μm laser spot on the sample. The exciting source was a 457.9 nm Ar^+ laser line. The Raman spectra of the 20% BSG sample are shown in Fig. 4. Using the iterated Lorentzian fitting to the spectrum, three peaks were obtained and shown by dash curves. The sources of the peaks are indicated by dotted lines and arrows in the figure. For the as-grown 20% sample without etching, as shown in (a), three peaks around 513, 516, and 521.5 cm^{-1} are observed. For the sample after some etching, as shown in (b), the peak positions are similar. However, the intensity ratio of the 516 cm^{-1} peak to other peaks decreases. The 513, 516, and 521.5 cm^{-1} peaks were assigned to the SiGe layer, the strained 5 nm Si cap layer on the top of the SiGe layer and the bulk Si substrate under the BSG layer, respectively. Due to the etching of the top Si layer, the relative intensity of the 516 cm^{-1} peak decreases. After some more etching, as shown in (c), peaks around 513 and 521.5 cm^{-1} do not shift, while the peak around 516 cm^{-1} shifts to about 518.5 cm^{-1}. After even more etching, as shown in (d), the intensity ratio of the 513 cm^{-1} peak to other two peaks drops significantly. The peak at 518.5 cm^{-1} was assigned to the strained thin Si substrate beneath the SiGe layer. With the etching of the top Si cap layer, the peak appeared. With the etching of the SiGe layer, the intensity of this peak increased. The as-grown 5% BSG sample was measured in the same way. There were only two peaks which were around 513 and 521.5 cm^{-1} for all samples. This further confirmed that the peak around 518.5 cm^{-1} came from the strained thin Si layer beneath the SiGe layer. Using the formula from the literature, the strain in the thin Si layer was calculated from the shift of the Si–Si peak $\Delta\omega_{Si-Si}$.[17] For the 3 cm^{-1} shift $\Delta\omega_{Si-Si}$, using $\Delta_{Si}=34$ cm^{-1}, the normalized strain Σ is $\Delta\omega_{Si-Si}/\Delta_{Si}=0.088$. As the full (100%) mismatch strain between pure Ge and pure Si makes $\Sigma=1$, considering the Ge composition 0.25, the normalized strain in the thin Si layer was 0.088/0.25=35.2%. Assuming the strain of the Si layer accommodated all the relaxation of the SiGe layer, then the relaxation of the SiGe layer was about 1%–35.2%=64.8%. This value matches very well with the 64% relaxation obtained from the DAXRD measurement. Therefore, the thin Si layer of the 20% BSG substrate worked as a compliant substrate to accommodate part of the mismatch strain since the BSG was soft at the growth temperature.

In summary, an effective compliant substrate was fabricated by forming 20% concentration B_2O_3 borosilicate glass in a SOI wafer and thinning down the Si layer on top of the borosilicate glass. It was demonstrated that the compliant substrate accommodated part of the misfit strain between the SiGe layer and the Si layer during the growth. This kind of substrate therefore has the potential to provide low dislocation density growth of relaxed SiGe layers for device applications.

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