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## Study on Thermal Oxidation of Si Nanowires

J. L. LIU, Y. LU, Y. SHI, S. L. GU, R. L. JIANG, F. WANG, H. M. BU,  
and Y. D. ZHENG

*Department of Physics and Institute of Solid State Physics, Nanjing University,  
Nanjing 210093, People's Republic of China*

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In this paper we reported the results on the low-temperature thermal oxidation of Si nanowires. Various polygon-shaped Si nanowires with linewidths between 100 and 300 nm were fabricated on Si/Si<sub>1-x</sub>Ge<sub>x</sub>/Si heterostructure substrates by using lithography, reactive ion etching, and subsequent selective chemical etching. We find that oxidized Si nanowires following 750 and 775 °C wet oxidation will keep the same shape as the initial unoxidized samples, and all the SiO<sub>2</sub> boundaries of oxidized samples will arrive at a circular shape. These results, which should be due to stress effects, provide useful information for understanding the behavior of non-planar oxidation that is used in modern Si nanoelectronic technology.

### 1. Introduction

As device sizes in modern very large scale integration (VLSI) technology continue to be reduced, the thermal oxidation of Si nanostructures is becoming increasingly important since it plays an important role in electrical isolation with trenches and local oxidation. In recent years, much interest has been attracted by the fabrication of SiO<sub>2</sub>-coated Si nanowire field-effect transistors due to the possibility of obtaining new and novel transport properties [1, 2]. This kind of transistors has many remarkable advantages, for example, Si nanowires are produced with both smooth Si/SiO<sub>2</sub> interface boundaries and controllable lateral dimensions by precisely controlling the oxidation process; electrons or holes are completely confined since SiO<sub>2</sub> acts as a high potential barrier. As a result, understanding of the thermal oxidation of Si nanowires is very important in modern VLSI technology.

Early work on the two-dimensional oxidation of Si nanostructures by Marcus and Sheng [3] indicates that greatly reduced oxide growth lies in the corners of Si trenches. Then, the two-dimensional oxidation process was studied experimentally and theoretically by Kao et al. [4] for patterned Si cylinders with diameters larger than 1 μm, by us for Si nanowires with linewidths ranging from 40 to 300 nm [5], and by Liu et al. [6] for Si columns with dimensions below 10 nm. All these works indicate that the oxidation rate of Si nanowires decreases due to the associated stress arising from the nonplanar viscous deformation of oxide, and that the retardation is more severe for smaller radii of Si nanowires and at lower oxidation temperatures. As seen from these papers, the interest has mainly been focused on the oxidation of cylindrical structures of controlled curvature, radii and up to now little work was being done based on Si nanowires with other cross-sectional shapes [7, 8].

## 2. Experimental Procedure

In this paper, we reported on the low-temperature wet oxidation of various polygon-shaped Si nanowires with linewidths between 100 and 300 nm. The fabrication of polygon-shaped Si nanowires consists of Si/Si<sub>1-x</sub>Ge<sub>x</sub>/Si heteroepitaxy, lithography, reactive ion etching and subsequent selective chemical etching. All the nanowires were oxidized at temperatures below 800 °C and the oxide morphology was studied by a scanning electron microscope (SEM). We find that oxidized Si nanowires following 750 and 775 °C wet oxidation still keep the same shape as the initial unoxidized samples. Moreover, all the SiO<sub>2</sub> boundaries of oxidized samples will arrive at a circular shape. These new phenomena which were not found in earlier works provide useful information for understanding and predicting the behavior of nonplanar oxidation that is used in many modern electronic devices.

The starting materials was a (100)-oriented p-type Si wafer with a resistivity of 25 to 50 Ωcm. First, the substrate was cleaned chemically by a modified Shiraki procedure [9]. A Si/Si<sub>1-x</sub>Ge<sub>x</sub>/Si heterostructure film was grown by very low pressure chemical vapor deposition (VLP-CVD) using SiH<sub>4</sub> and GeH<sub>4</sub> as source gases. Here, a 100 nm thick Si buffer layer was grown on the Si substrate, followed by the growth of the Si/Si<sub>1-x</sub>Ge<sub>x</sub> layer. On top of the Si/Si<sub>1-x</sub>Ge<sub>x</sub> layer, a high-quality superficial Si layer was deposited. Subsequently, mask and lithography techniques were carried out to generate line-and-space patterns along the (110) direction on the Si/Si<sub>1-x</sub>Ge<sub>x</sub>/Si heteroepitaxial film. The trenches were formed by reactive ion etching using SF<sub>6</sub> gas. Next, the selective chemical etching was performed with the HNO<sub>3</sub>:CH<sub>3</sub>COOH:diluted HF solution to etch the trench structures in order to remove the Si/Si<sub>1-x</sub>Ge<sub>x</sub> layers and form the Si wires. After removing the resist, the as-etched Si wires were thermally oxidized below 800 °C in wet oxygen atmosphere. As illustrated in Fig. 1, it is expected that the

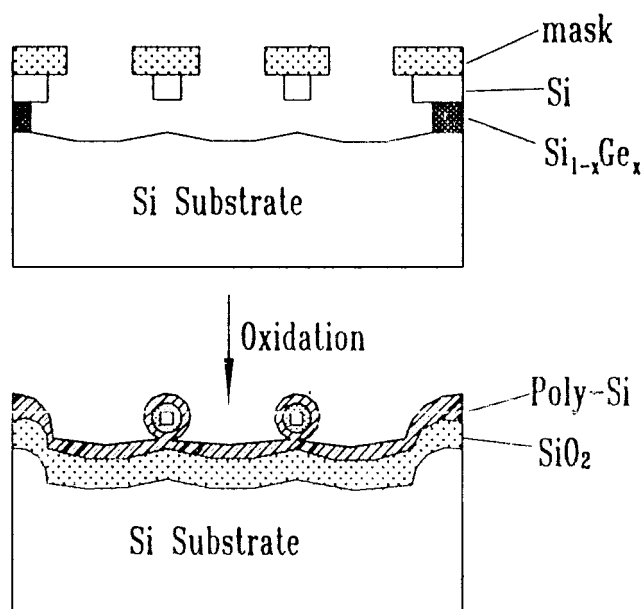


Fig. 1. Schematic diagram of square-shaped Si nanowire structures: upper part: before oxidation, and lower part: after low-temperature oxidation. Here, the outer poly-silicon film mask was used to clearly distinguish the oxide morphology in the SEM image, as shown in the following figures

Si core of the oxidized sample will still keep its square shape and the  $\text{SiO}_2$  boundaries form circular shapes even though the linewidth of the wires decreases dramatically.

In this fabrication process, the selective chemical wet etching conditions are very important in generating various polygon-shaped Si nanowires on  $\text{Si}/\text{Si}_{1-x}\text{Ge}_x/\text{Si}$  hetero-epitaxial films. It was demonstrated that  $\text{HNO}_3:\text{CH}_3\text{COOH}:\text{diluted HF}$  was very good in reducing SiGe nanostructures [10]. Furthermore, the optimum etch rate and selectivity are well obtained by altering the etchant composition and Ge fraction. Here, by controlling the ratio of the constituents of the etchant, the Ge fraction in the  $\text{Si}_{1-x}\text{Ge}_x$  layer, and other etching conditions such as temperature etc., Si wires with various cross-sectional shapes such as squares, triangles, rectangles and pentagons were easily achieved.

### 3. Results and Discussion

Fig. 2b shows the cross-sectional SEM image of the oxidized quasi-square Si wires. It is produced at  $750^\circ\text{C}$  wet oxidation for 6 h. Protective polycrystalline Si deposited by a VLP-CVD reactor appears as outer layer in order to clearly distinguish the oxide and interface morphology. As shown in Fig. 2b, the oxidized wire still retains square shape. In addition, the oxide surfaces away from the corners of the quasi-square wire are nearly of the same thickness, and  $\text{SiO}_2$  on the four flat surfaces of the quasi-square wire are thicker than that around the corners. Moreover, the  $\text{SiO}_2$  surface has arrived at a circular shape.

SEM photographs of cross-sections through other oxidized Si nanowires are shown in Fig. 3. Fig. 3a is an oxidized rectangular-shaped sample which is oxidized at  $775^\circ\text{C}$  in

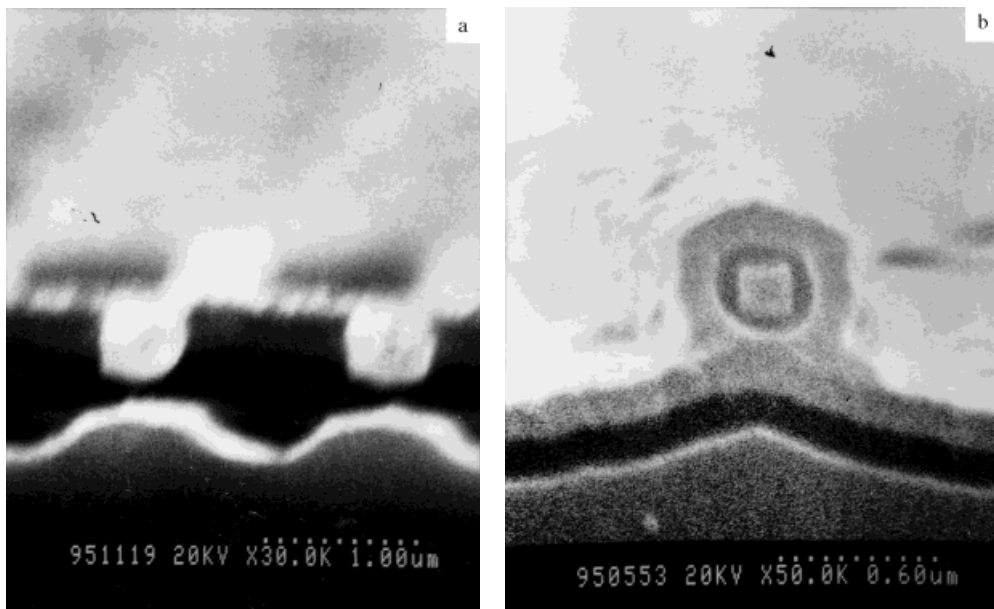


Fig. 2. Comparison between two cross-sectional SEM images of a) as-etched quasi-square Si nanowires prepared by selective chemical etching, and b) the oxidized quasi-square Si wires after 6 h  $750^\circ\text{C}$  wet oxidation

wet oxidation for 12.5 h. It is seen that the outer surface of the oxide has arrived at a circular shape, and the shape of the wire remains rectangular. In addition, an unexpected and exciting result is obtained by measuring the oxide thickness on the (110) and (100) surfaces of the wire. From Fig. 3a, the oxide thickness on the (110) and (100) surfaces of the wire are about 180 and 300 nm, respectively. These data show that the oxidation rate of the (100) surfaces of the wires is faster than of the (110) surface,

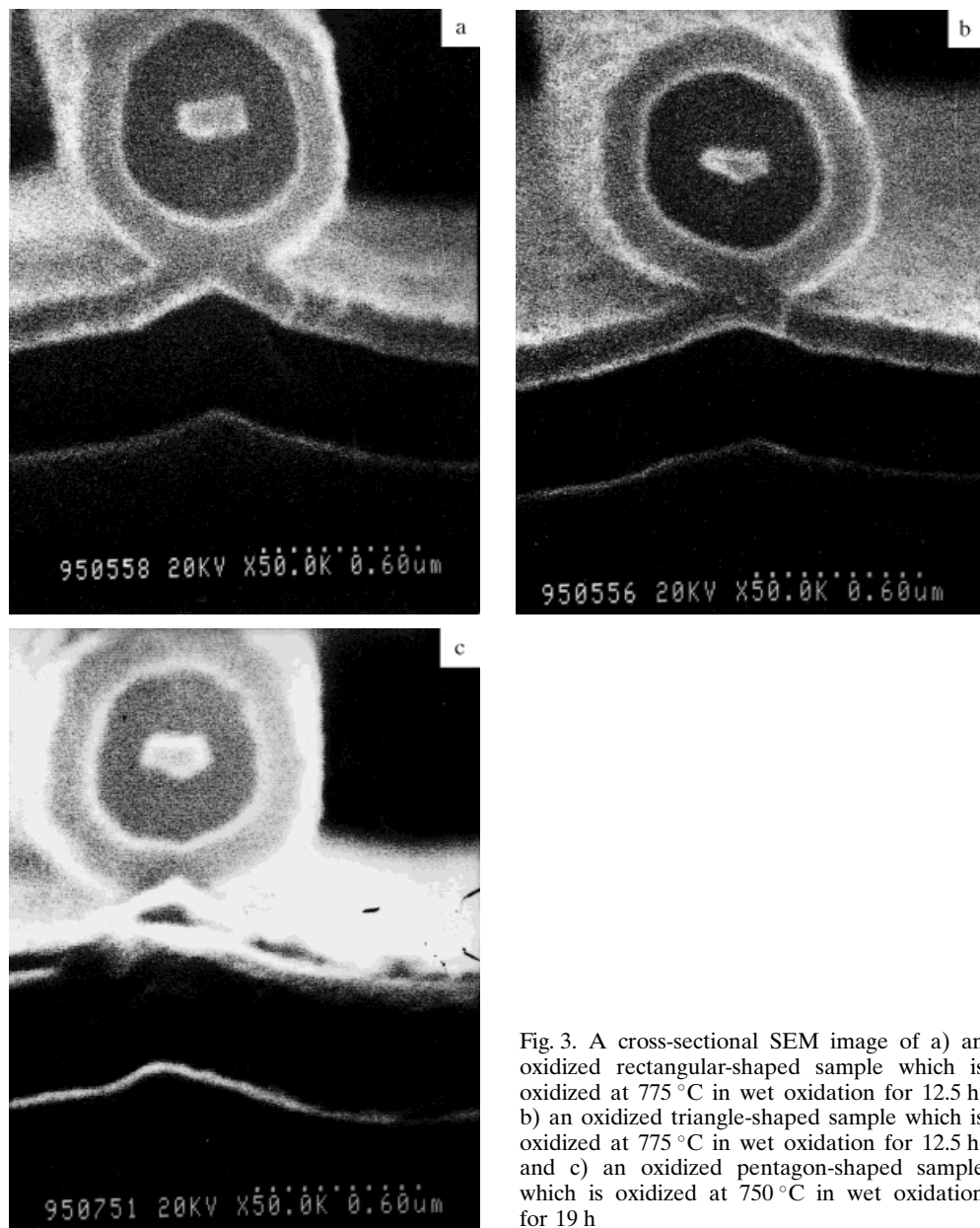


Fig. 3. A cross-sectional SEM image of a) an oxidized rectangular-shaped sample which is oxidized at 775 °C in wet oxidation for 12.5 h, b) an oxidized triangle-shaped sample which is oxidized at 775 °C in wet oxidation for 12.5 h, and c) an oxidized pentagon-shaped sample which is oxidized at 750 °C in wet oxidation for 19 h

which is in agreement with the result reported by other authors [3]. Fig. 3b is an oxidized triangular-shaped sample which is oxidized at 775 °C in wet oxidation for 12.5 h. Fig. 3c is an oxidized pentagonal-shaped sample which is oxidized at 750 °C in wet oxidation for 19 h. Oxidation results similar to that of square wires occurred in these wires, that is, outer surfaces of the oxide form a circular shape in these cases, and the shapes of the nanowires retain their initial shapes.

Two-dimensional thermal oxidation of cylindrical Si wires has already been studied thoroughly [4 to 6]. Oxidation retardation related to oxide viscous stress in Si wires has been demonstrated. For the present oxidation of various polygon-shaped Si nanowires, additional complexities are introduced to the problem of oxidation. As the oxidation progresses, oxidant diffusion in the deformed oxide, viscous flow of oxide, and stress arising from nonplanar viscous deformation of SiO<sub>2</sub> are more complex compared with that in the oxidation of cylindrical Si wires. In addition, effects of different crystal orientations of a curved Si surface on the local oxidation rates cannot be omitted. Here, we supposed that the present oxidation of various polygon-shaped Si wires consists of two parts, one is the two-dimensional oxidation at the corners, the other is the one-dimensional oxidation at the flat surface of the nanowires. The underlying physical mechanism of oxidation at the flat surface is based on the Deal-Grove model [10]. The oxidation retardation at the corners observed above can usually be contributed to the additional normal stress arising from the nonplanar viscous deformation of the oxide [4 to 6]. The normal stress makes the oxide growth at the corners greatly reduced while the Si species at the flat surfaces continue to be oxidized. In addition, tangent viscous flow of the oxide may also occur due to large tensile stress at the corners. All these factors lead to the unchangeable shape of the wire and final circular SiO<sub>2</sub> boundaries. Though we can suppose that the stress effect is essential for the present low-temperature oxidation, further data must be taken before exact conclusions and interpretation can be made.

#### 4. Conclusion

In summary, we studied wet oxidation of square-, triangle-, rectangle-, pentagon-shaped Si nanowires. These nanostructures have been fabricated by using lithography, reactive ion etching, and subsequent chemical etching. The nanowires are wet oxidized at temperatures below 800 °C. We find that oxidized samples will still keep the same shape as the initial unoxidized samples in all cases, and all the SiO<sub>2</sub> boundaries of the oxidized samples will arrive at a circular shape. These oxidation phenomena should be due to stress effects.

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