Fabrication of silicon nanowires

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Abstract. Pentagon-shaped silicon wires with linewidth around 300 nm are successfully fabricated by using the Si/SiGe epitaxy technique, reactive ion etching, and subsequent selective chemical etching. The nanowires are oxidized in wet O_2 at 750 °C and 850 °C. The oxide and interface morphology are characterized by cross-sectional scanning electron microscope images. It is found that the oxidized nanowire following oxidation at 750 °C still keeps its pentagon shape even if it has been oxidized for 19 h. However, the oxidized samples at 850 °C become circular in shape. The oxidation-temperature dependence of the sample shapes is discussed. Our results should be useful in generating silicon nanowires coated with SiO_2 in microelectronic technology with careful selection of the SiO_2 growth temperatures.

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Field-effect devices having SiO_2-coated silicon nanowires acting as trenches have recently received great attention, since new physical phenomena with applications in future very-large-scale integration (VLSI) devices are expected [1, 2]. Transport properties in these devices depend on the size and shape of the silicon wires. As a result, study of the thermal oxidation of silicon nanowires of various sizes and shapes, as a key process in fabricating SiO_2-coated silicon nanowire field-effect devices, is very important.

Up to now, much interest has been focused on the oxidation of silicon cylinders. Early work was done by Kao et al. with silicon cylinder diameters larger than 1 μm [3]. Oxidation of silicon cylindrical structures has also been studied by J.L. Liu et al. with silicon wire linewidths ranging from 40 nm to 250 nm [4], and by H.I. Liu et al. with silicon columns of dimensions below 10 nm [5]. In addition, other authors have studied oxidation of triangle-shaped silicon nanowires [6, 7]. All these works have provided a controllable way of defining the size and shape of silicon nanowires, which is very useful in fabricating expected silicon nanowire field-effect devices. At the present stage, there is still an urgent need to obtain oxidation results for silicon nanowires of other shapes.

It is well known that SiGe/Si heteroepitaxial film is very useful in fabricating various silicon wires and related devices because of its excellent properties, such as high-quality epitaxial growth, selective etching, and thermal oxidation. Recently, formation of silicon quantum wires with the physical boundaries of SiO_2 based on a SiGe heterostructure have been reported [4]. Here, we describe the fabrication and oxidation of pentagon-shaped Si nanowires. This process was done by first growing a high-quality $Si/Si_{1-x}Ge_x/Si$ heteroepitaxial film on a Si substrate by very low pressure chemical vapor deposition (VLP/CVD), followed by lithography and reactive ion etching to form trench structures. Subsequently, the selective chemical wet etching with a solution of HNO_3:CH_3COOH:diluted HF was used to remove the $Si_{1-x}Ge_x$ layer and form pentagon-shaped silicon wires. Finally, thermal oxidation in wet O_2 was carried out and the oxide morphology was characterized by scanning electron microscopy (SEM). The thermal oxidation of pentagon-shaped wires will be discussed.

Figure 1a is a schematic of a pentagon-shaped silicon wire structure. The structure was generated as follows. The silicon substrate was a $\langle 100 \rangle$-oriented p-type silicon wafer with a resistivity of 25–50 Ω cm. First, a Si/SiGe/Si layer was deposited on the substrate by VLP/CVD with SiH_4 and GeH_4 as the gaseous sources. It started with a Si buffer layer of 100 nm, followed by a graded $Si_{1-x}Ge_x$ layer of 200 nm with the Ge content x decreasing linearly from 0.2 to 0. High-quality superficial silicon layer was deposited on top of these strain adjusting layers. Then, masks with line-and-space patterns parallel to the $\langle 110 \rangle$ direction were lithographically defined on the $Si/Si_{1-x}Ge_x/Si$ epitaxial film. The trench structures were generated by reactive ion etching using SF_6 gas. Next, the substrate was dipped into HNO_3:CH_3COOH:diluted HF in order to create the silicon nanowires. Note that the selective chemical etchant HNO_3:CH_3COOH:diluted HF was very effective in reducing SiGe nanostructures, and a higher etch rate is obtained by increasing the Ge content in the $Si_{1-x}Ge_x$ layer [8]. As a result, for the present graded $Si_{1-x}Ge_x$ layer, the etch rate at the bottom layer of the $Si_{1-x}Ge_x$ is higher than that at the upper
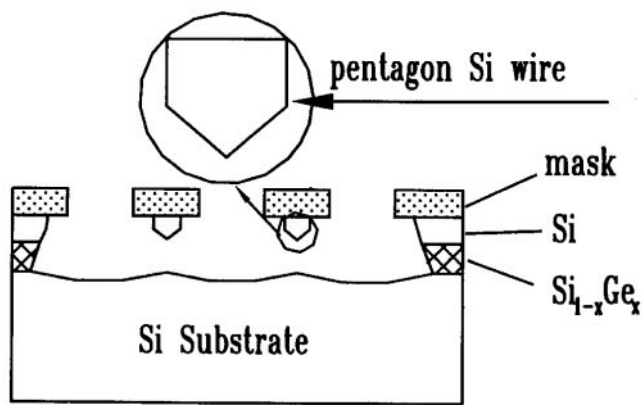
Fig. 1. a Schematic of pentagon-shaped silicon wires. **b** Cross-sectional SEM image of as-etched pentagon-shaped silicon nanowires prepared by the selective etching

layers, and after a suitable etch time, pentagon-shaped silicon nanowires can easily be obtained.

Figure 1b shows a cross-sectional SEM image of as-etched pentagon-shaped silicon nanowires prepared by selective etching. Here, the ratio of the $HNO_3:CH_3COOH$:diluted HF etchant is chosen as 40:15:1. The pentagon-shaped silicon wires were formed by dipping the $Si/Si_{1-x}Ge_x/Si$ trench structure in the etchant for 120 s. As can be seen, the wires are smooth and isolated from the substrate.

Figure 2 shows a cross-sectional SEM image of the oxidized samples produced in wet oxidation at (a) 750 °C after 19 h, (b) 850 °C after 6 h, and (c) 850 °C after 12.5 h. Here, protective polycrystalline silicon deposited by the VLP/CVD reaction appears as the outer layer in order to distinguish clearly between the oxide and interface morphology. As can be seen in Fig. 2, the nanowires oxidized at 750 °C still keep the same shape as the initial pentagon even though the linewidth decreased dramatically after 19 h. However, the sample oxidized at 850 °C becomes circular in shape after 6 h. When the oxidation time is increased to 12.5 h (Fig. 2c), the diameter of the wire is reduced to 40 nm.

These oxidation characteristics seem interesting, and may be understood by considering the stress effect in the oxidation. The underlying mechanism in a wet oxidation of silicon is the diffusion of oxidant through the already-formed oxide layer to react with Si at the interface and form SiO_2. For
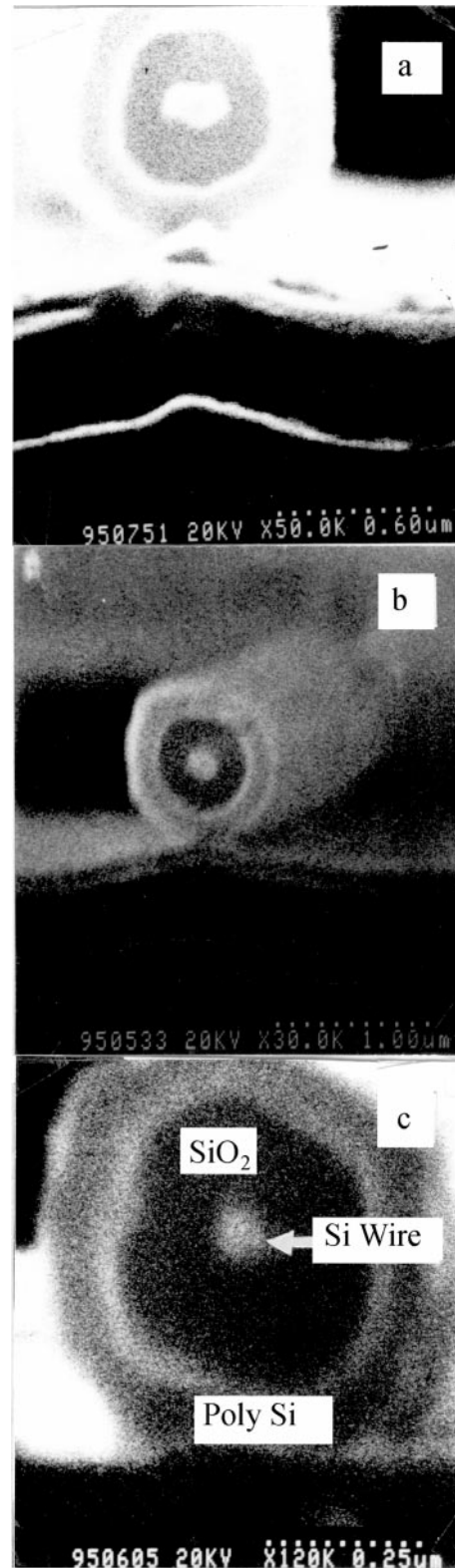

Fig. 2a–c. Cross-sectional SEM image of the oxidized pentagon-shaped silicon wires produced in wet oxidation at **a** 750 °C after 19 h, **b** 850 °C after 6 h, and **c** 850 °C after 12.5 h

the wet oxidation of pentagon-shaped silicon wires at 750 °C, nonplanar deformation of the oxide at the corners causes a stress normal to the interface and a tensile stress parallel to the interface. On the one hand, it is the local normal stress on the local solubility of oxidant in SiO_2 and the surface re-
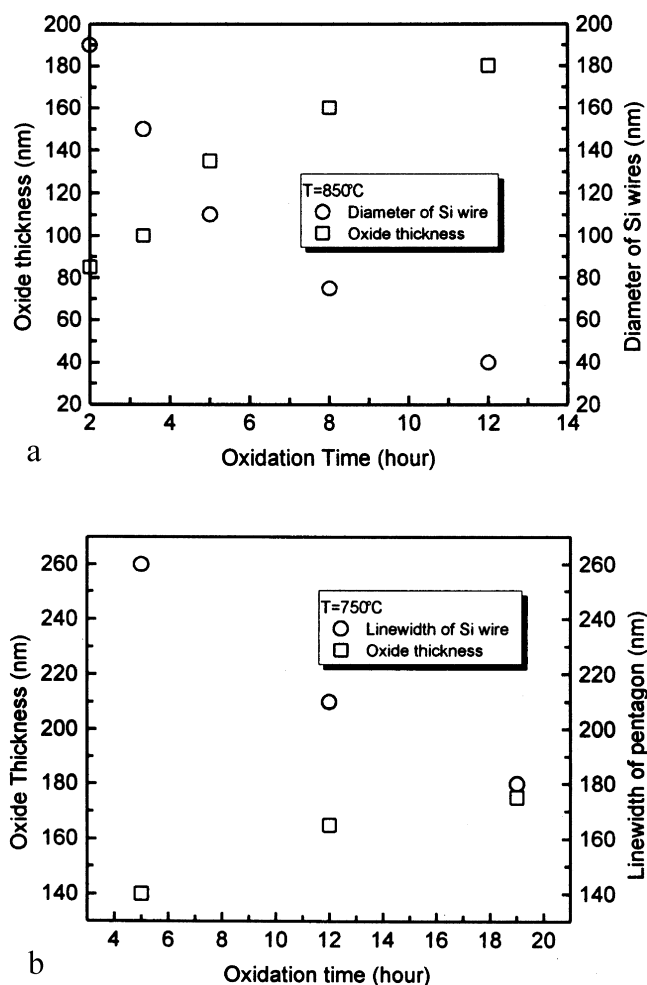
Fig. 3a,b. Oxide thickness and linewidth as a function of the oxidation time for **a** 850 °C, the left vertical axis is oxide thickness on the silicon wires and the right vertical axis is diameter of silicon wires, and **b** 750 °C, the left vertical axis denotes oxide thickness on the upper side of the pentagon silicon nanostructure and the right axis denotes linewidth of the upper side of the pentagon

graphs. Figure 3 shows the oxide thickness and linewidth as a function of the oxidation time for (a) 850 °C, where the left vertical axis is the oxide thickness on the silicon wires and the right vertical axis is the diameter of the silicon wires, and (b) 750 °C, where the left vertical axis denotes the oxide thickness on the upper side of the pentagonal silicon nanostructure and the right axis denotes the linewidth of the upper side of the pentagon. As the oxidation progresses, oxidation retardation of silicon wires is observed at the two temperatures. The retardation of oxidation depends strongly on the oxidation temperatures. It is more pronounced at 750 °C. After 19 h of oxidation at 750 °C, the retardation rate of the linewidth becomes extremely small. This phenomenon is not observed for wet oxidation at 850 °C, and it is confirmed that all the circular wires vanish after 16 h. The trend of the oxide thickness data shows that the SiO_2 growth rate decreases with the increase in the oxidation time for the two temperatures and the oxide thickness appears to saturate to an asymptotic value of 180 nm in both cases.

In summary, we have reported on the fabrication and wet oxidation of pentagon-shaped silicon nanowires. The fabrication process consists of $Si/Si_{1-x}Ge_x/Si$ epitaxy, reactive ion etching, and subsequent selective chemical etching. The nanowires are oxidized in wet oxygen at 750 °C and 850 °C, and the oxide and interface morphology are characterized by SEM. It is found that the oxidized nanowire following 750 °C oxidation still keeps the pentagon shape even if it has been oxidized for 19 h. However, the samples oxidized at 850 °C become circular after 6 h. The behavior of the oxidation at 750 °C and 850 °C shows that as the oxidation progresses, oxidation retardation of silicon wires is observed at these temperatures. Moreover, the retardation of oxidation depends on the oxidation temperature. The lower the temperature is, the more pronounced is the observed retardation. In addition, the oxide thickness appears to saturate to similar asymptotic values in both cases.

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action coefficient that retard the oxidation at the corners. On the other hand, because of the appearance of tensile stress in the oxide, the transport of oxidants is enhanced. These two conflicting factors seem to reach an equilibrium in which, as oxidation progresses, the oxidation rate of five faces of the pentagon structure is equal to that at the corners. As a result, no obvious shape change in the pentagon structure occurs though the dimension is reduced to a very small value. As the oxidation temperature is raised to 850 °C, the oxide viscosity decreases and the magnitude of the stress becames less. In addition, viscous oxide can flow elsewhere easily as a result of the relief of stress [9]. Hence, the equilibrium should be broken, the corners are oxidized faster than the five faces of the pentagon, and a shape change is observed.

Oxidation results for 850 °C and 750 °C at different oxidation times have been investigated. Prior to the thermal oxidation, a set of samples are prepared under the same etching conditions to minimize variations in the silicon wires among the samples. All data are obtained from the SEM micro-