HOLE TRANSPORT PROPERTIES OF $Si / Si_{1-x}Ge_x$ MODULATION–DOPED HETEROSTRUCTURES

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We report hole transport properties of p–type $Si / Si_{1-x}Ge_x$ modulation –doped heterostructures grown with rapid thermal processing very low pressure chemical vapor deposition (RTP–VLP CVD) at temperatures ranging from 293K to 77K. Hole mobilities as high as 300 $cm^2V^{-1}s^{-1}$ at 293K, and 8400 $cm^2V^{-1}s^{-1}$ at 77K for $x = 0.3$, have been achieved. The effects of Ge content and the thickness of Si spacer layer on the hole mobility are studied.

1. Introduction

It is well known that modulation doped Si / SiGe heterostructures have become increasingly important for the fabrication of high speed device applications such as the Si / SiGe modulation–doped field–effect device. High electron mobility n–type Si / SiGe modulation doped heterostructures and high hole mobility p–type Si / SiGe modulation–doped heterostructures have been reported [1–4]. In this paper, we present the transport properties of p–type $Si / Si_{1-x}Ge_x$ modulation–dope heterosturctrues by RTP–VLP CVD in the temperature range from 293K to 77K, desired for device application. It was found that the hole mobility increased strongly with decreasing temperature. A high hole mobility, 8400 $cm^2V^{-1}s^{-1}$, has been achieved for a sheet carrier concentration of $1.2 \times 10^{13} cm^{-2}$ at 77K. The effects of Ge content and the thickness of Si spacer layer on the hole mobility are studied.

2. Experimental

The $Si / Si_{1-x}Ge_x$ P–type modulation–doped (MD) heterostructures were grown with different x ($x = 0.2$, 0.25, 0.3) values on (100) silicon wafers by RTP–VLP CVD. Details of the growth system have been reported earlier [5]. The heating source is a tungsten –hologen lamp which is used as a "thermal switch" to turn the CVD reaction on and off. SiH_4, GeH_4 and B_2H_6 are used as reactive gases and doping gases, respectively. All process parameters and sequences are controlled by computer. The operating pressure is $10^{-3} \sim 10^{-2}$ torr, and the growth temperature was 600℃. The growth rate was as low as 0.1nm / sec.

Prior to growth, the Si wafers were cleaned by the RCA process [6], followed by a dilute HF dip which resulted in a H–terminated surface.

Fig.1 shows the schematic for a $Si / Si_{1-x}Ge_x / Si$ p–type modulation–doped double heterostructure. P^+–Si doping layers of 20nm thickness were doped with boron to $1–3 \times 10^{19} cm^{-3}$, and $Si_{1-x}Ge_x$ strained layers of 40nm thickness were not intentionally doped. The thickness of undoped Si spacer layer is 15nm.

For comparison, uniformly doped (UD) Si /

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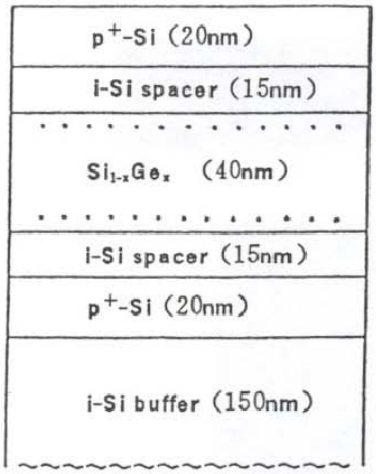

Fig. 1. Schematic for $Si / Si_{1-x}Ge_x / Si$ p-type modulation-doped double heterostructure

$Si_{1-x}Ge_x$ heterostructures were also grown under the same growth conditions. The $Si_{0.8}Ge_{0.2}$ layers of 180nm thickness were doped with boron to $1-3 \times 10^{19}cm^{-3}$.

3. Results

The electrical characterization was performed using Hall-Van der Pauw measurements in the range 293-77K, as desired for device applications. The mobility and sheet hole concentration values are shown in Table 1. It was found that the hole mobility of p-type modulation-doped $Si / Si_{1-x}Ge_x$ heterostructures is higher than that of bulk silicon. For indentical sheet carrier concentration, at room temperature, these hole mobilities are more than six times larger than those

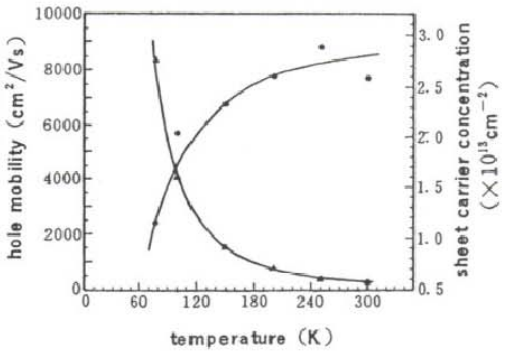

Fig. 2. Temperature dependence of hole Hall modility and sheet carrier concentration for $Si / Si_{0.7}Ge_{0.3} / Si$ p-type modulation-doped double heterostructure

achievable in bulk doped Si. (See Table 1, sample No.5.) Low temperature hole mobility enhancement was observed in all MD samples. The peak hole mobility is 300 $cm^2V^{-1}s^{-1}$ at 293K and increases to 8400 $cm^{-2}V^{-1}s^{-1}$ at 77K for $x = 0.3$. The low temperature hole mobility of MD samples is much higher than that of UD sample No.4. This is evidence of carrier separation from parent impurities due to the valence band offset.

The hole mobility and sheet hole concentration as a function of temperature for a $Si / Si_{0.7}Ge_{0.3} / Si$ MD heterostructure is shown in Fig.2. The hole mobility increases with decreasing temperature, because the lattice scattering decreases and the influence of remote ionized impurities scattering is very small. The decrease of sheet carrier concentration at low temperature indicates that some of the holes have been frozen out.

Fig.3 shows the dependence of hole mobility on Ge fraction x for MD heterostructures. Both at room

Table 1. Hall data for MD and UD samples at 293K and 77K.

Sample			$P_s(\times 10^{13}cm^{-2})$		$\mu_H(cm^2/V \cdot s)$	
No.	Ge fraction	MD / UD	293K	77K	293K	77K
1	$x = 0.2$	MD	6.6	2.2	240	5300
2	$x = 0.25$	MD	6.7	2.3	280	7500
3	$x = 0.3$	MD	2.6	1.2	300	8400
4	$x = 0.2$	UD	6.5	7.3	210	130
5	$x = 0$	UD	$2.1 \times 10^{19}cm^{-3}$	$3.1 \times 10^{19}cm^{-3}$	38	26

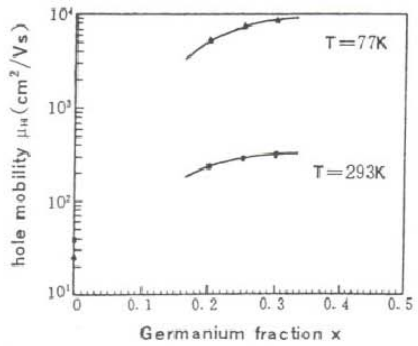

Fig. 3. Hole Hall Mobility VS Ge fraction at 293K and 77K for Si / $Si_{1-x}Ge_x$ / Si p–type modulation –doped doulbe heterostructure

temperature (293K) and low temperature (77K) the hole mobility increases with increasing x. The primary reason is that the hole effective mass decreases with the increment of Ge content, which is in agreement with the results of theoretical calculations [7].

In the design of sample structures, the thickness of spacer layers is very important, because the low temperature hole mobility is most probably limited by remote ionized impurity scattering from the p^+–Si layer and B segregation into the SiGe channel, as show in Fig.1. The effects of the thickness of the Si spacer layer on the hole mobility was studied. Our results show that a 15nm spacer layer thickness is optimal for producing maximum hole mobility in the range of 300–77K.

4. Summary

High hole mobility p–type Si / $Si_{1-x}Ge_x$ modulation–doped heterostractures have been successfully grown on silicon substrates by RTP–VLP CVD. The hole mobility was as high as 300 $cm^2V^{-1}s^{-1}$ at 297K, and 8400 $cm^2V^{-1}s^{-1}$ at 77K. It was found that the hole mobility is apparently enhanced by decreasing temperature, and also increases with increasing Ge content.

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