A method for fabricating silicon quantum wires based on SiGe/Si heterostructure

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(Received 2 August 1995; accepted for publication 30 October 1995)

A method for fabricating silicon quantum wires with SiO_2 boundaries is presented. It is accomplished by first growing Si/SiGe/Si heterostructure on silicon substrate with very low-pressure chemical vapor deposition, followed by lithography and reactive ion etching to form trench structures. Finally, the selective chemical etching of SiGe over silicon and subsequent thermal oxidation are carried out to generate expected silicon quantum wires. The result observed is demonstrated using scanning electron microscopy. Furthermore, the thermal oxidation characteristics of the silicon wires are investigated. The present method provides a well-controllable way to fabricate silicon quantum wires and is fully compatible with silicon microelectronic technology. © *1996 American Institute of Physics.* [S0003-6951(96)01103-5]

Silicon-based low-dimensional structures such as silicon quantum wires (SQWRs) have recently attracted great interest both for potential device applications and for novel physical phenomena. Obviously, it is essential to fabricate SQWRs in a well-controllable way. In contrast with the GaAs/AlGaAs system, however, only a few fabrication methods have been reported. Most of SQWRs were obtained using metal–oxide semiconductor (MOS) structures, where carrier confinement was achieved by electrostatic potential.[1–3] Several authors recently reported methods of fabricating physically confined SQWRs with SiO_2 boundaries by anisotropic chemical etching and thermal oxidation.[4–7] At present, there still exists an urgent need for the development of advanced fabrication techniques for obtaining high-quality SQWRs.

SiGe/Si heteroepitaxial film has many potential applications in silicon technology. It would be very useful to apply this film to the fabrication of SQWRs and related devices due to its excellent properties such as high-quality epitaxial growth, selective etching, and thermal oxidation. Usami *et al.* successfully fabricated arrays of SiGe quantum wires on a v-groove patterned silicon substrate by gas-source silicon molecular beam epitaxy.[8] Recently, we realized SiGe/Si multiple quantum well wires using selective chemical etching technique.[9] In this letter, a novel method for fabricating the physically confined SQWRs based on SiGe/Si heterostructure is presented combining SiGe/Si heteroepitaxy, selective chemical wet etching, and subsequent thermal oxidation. Here, high-quality Si/SiGe/Si heteroepitaxial film is first grown on silicon substrate. On the trench structures generated by lithography and reactive ion etching, the selective chemical wet etching is utilized to remove the SiGe layer and form silicon wires. Finally, the thermal oxidation process is carried out to obtain expected SQWRs with SiO_2 boundaries. Thermal oxidation of silicon wires is one of the critical processes in fabricating the SQWRs, which not only forms high-quality SiO_2/Si interfaces, but also smooths and reduces the lateral dimensions of the SQWRs. Thus the lateral dimensions of the SQWRs can be well controlled by combining SiGe/Si heteroepitaxy, selective chemical wet etching, and subsequent thermal oxidation. Here, the thermal oxidation characteristics of silicon wires are investigated. The result observed is demonstrated using scanning electron microscope (SEM).

The fabrication step is illustrated in Fig. 1. First, a $Si_{0.8}Ge_{0.2}$ heteroepitaxial layer was grown on ⟨100⟩ oriented *p*-type 25–50 Ω cm silicon substrate by very low-pressure chemical vapor deposition (VLP-CVD). The details of the growth technique have already been reported elsewhere.[10] The thickness of the $Si_{0.8}Ge_{0.2}$ layer was 100 nm, while a buffer silicon layer of 100 nm was grown between the substrate and the SiGe layer. A silicon active layer was grown on

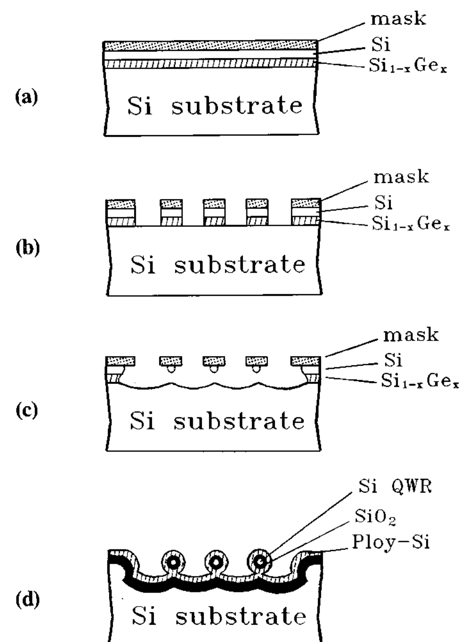

FIG. 1. Fabrication step of SQWRs: (a) Si/SiGe/Si heteroepitaxy by VLP/CVD; (b) mask pattern and shallow trench formation; (c) selective chemical etching; and (d) thermal oxidation.

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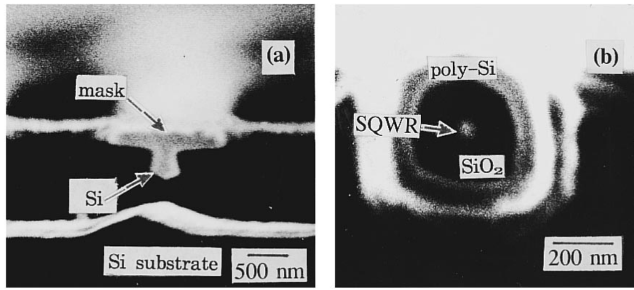

FIG. 2. Cross-sectional SEM image of (a) an as-etched silicon wire and (b) thinned SQWR with the linewidth of 40 nm.

the top of the $Si_{0.8}Ge_{0.2}$ layer [Fig. 1(a)]. A lithography technique was carried out to generate line-and-space patterns with periods of 1.0–2.0 μm here. Then, trenches were formed by using reactive ion etching (RIE) [Fig. 1(b)]. Next, the selective chemical etchant consisting of HNO_3:CH_3COOH:HF at 25 °C was used to etch the trench structures to remove $Si_{0.8}Ge_{0.2}$ layer out with the silicon wires remained [Fig. 1(c)]. After removing the mask, the silicon wires were thermally oxidized in wet oxygen atmosphere which smooths the surface of the silicon wires and reduces the lateral dimensions to form expected SQWRs. Finally, the thermal oxidation in dry oxygen was carried out to obtain high-quality SiO_2/Si interfaces [Fig. 1(d)].

Figure 2 shows a cross-sectional SEM image of SQWR. As seen from Fig. 2(a), a silicon wire is prepared by the selective chemical wet etching. The top layer above the silicon wire is the mask. In the last several years, the selective chemical etching techniques for SiGe/Si heteroepitaxial films have developed quickly. Among many selective chemical etchants, it has been demonstrated that the solution of HNO_3:CH_3COOH:HF was a very good etchant in thinning SiGe nanostructures without any defects and was often used.[9,11] The optimum etch rate and selectivity are easily obtained by altering the composition, and the selective etch ability increases with an increase in the mole fraction of Ge.[9,11] Through the selective chemical etching, the $Si_{0.8}Ge_{0.2}$ layer around the trench is removed and the silicon active layer is narrowed to form silicon wire. Subsequently, the interface of the silicon wire is smoothed and its lateral dimensions are reduced by thermal oxidation processes. Figure 2(b) shows the cross-sectional SEM image of a SQWR with circular cross section embedded in the SiO_2 after thermal oxidation. In order to clearly observe it, we deposit a polycrystalline silicon mask on the SQWRs by the VLP-CVD. We cut the sample to show the cross section and dip it in aqueous hydrogen fluoride for some time to isolate part of the SQWRs from the environment. As shown in Fig. 2(b), the lateral linewidth of the SQWR is about 40 nm here.

The advantage of using dry thermal oxidation to fabricate SQWRs has been demonstrated.[4,12] The self-limiting oxidation phenomena in silicon nanostructures was observed. It was seen as an opportunity for fabricating high-quality SQWRs with ± 1 nm control in lateral dimensions in the self-limiting regime of oxidation temperatures below 950°.[12] For the present SiGe/Si nanostructure, though the SiGe layer below the silicon wires is completely etched away after selective chemical etching, it still remains in another part of the sample. Hence, the oxidation at high temperatures is forbidden because of SiGe thermal stability. In addition, dry oxidation at low temperatures is not practical because of the length of time it takes to thin silicon wires to expected lateral dimensions. Fortunately, the wet oxidation at low temperatures offers a suitable opportunity for realizing SQWRs. Obviously, understanding the wet oxidation of silicon wires is important for fabricating well-controllable SQWRs. It is desired that the self-limiting oxidation effect observed in dry oxidation could also occur in the present wet oxidation. In the wet oxidation process, the flat surfaces oxidizes faster than silicon wires. As oxidation proceeds, the planar field oxide thickness continues to increase linearly with time, while the silicon wire oxide thickness increases slightly. This retardation of oxidation becomes obvious when the radius of the silicon wire is decreased. In addition, the retardation of oxidation also depends strongly on the oxidation temperature. In order to clarify the radius and temperature dependence of the retardation, experiments have been performed at three different oxidation temperatures of 850, 800, and 750 °C. All the samples used for the oxidation are prepared under the same etching condition to minimize silicon wire variations among samples. The typical starting radius of as-etched wires is about 120 nm. Dimensional data are obtained from the micrograph of SEM. These observations are plotted in Fig. 3. The vertical axis measures oxide thickness on silicon wire surfaces normalized to that on the flat surface, and the horizontal axis denotes the inverse of the radius of the silicon wire after oxidation. There is a general trend that the decrease of the lateral dimensions of silicon wires shows the retardation of oxidation for three oxidation temperatures as the oxidation progresses. However, the retardation of oxidation is more pronounced with decreasing the oxidation temperature. Oxide growth is severely retarded at 750 °C. The trend of the data for 750 °C indicates that the SQWRs seem nonvanishing, moreover, the final radius seems to be self-limited to 20 nm. This self-limiting oxidation phenomenon is

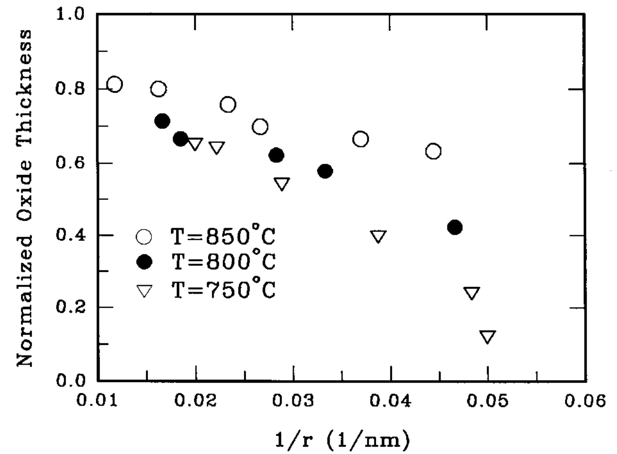

FIG. 3. Oxide thickness on SQWR surfaces normalized to that on the flat surface as a function of the inverse of the radius of the SQWRs for 850, 800, and 750 °C wet oxidation.

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not observed at 850 and 800 °C. It is confirmed that the SQWRs disappear after 14 and 20 h for 850 and 800 °C, respectively. The retardation of oxidation is usually attributed to the additional stress from nonplanar viscous deformation of oxide.[13] This viscous stress makes the oxidation reaction at the silicon surface more difficult. Based on the present observations, it is apparent that the extent of retard oxidation follows the change in the viscous stress with temperature and radius of silicon wires. It should be noted that the self-limiting oxidation phenomenon in wet oxidation is found to occur only for the temperature below 750 °C, which is about 200 °C lower than that in dry oxidation.[4] This may be due to the fact that the viscous stress of wet oxide is lower than that of dry oxide. There are two likely mechanisms for the slowing down of the oxidation rate. One is that the surface reaction coefficient K_s is reduced by the normal viscous stress at the Si/SiO_2 interface.[13] Another is that oxidation diffusion is limited in a highly stressed oxide.[4] Further studies are needed to identify the effects of the viscous stress on oxidation kinetic parameters.

In summary, we have successfully fabricated arrays of SQWRs with SiO_2 boundaries using the selective chemical etching of SiGe over Si and subsequent thermal oxidation technique based on Si/SiGe/Si heterostructure. Excellent results are evidenced by SEM. It is found that the lateral dimensions of SQWRs can be well controlled by the selective chemical etching and thermal oxidation process. We also find self-limiting oxidation phenomenon of silicon wires in wet oxidation at 750 °C. This research clearly shows the success of SiGe/Si heteroepitaxy, selective chemical wet etching, and thermal oxidation as a very valuable method for fabricating SQWRs.

The authors would like to acknowledge D. A. Du and C. Y. Lin of Center for Materials Analysis at Nanjing University for SEM measurement. Z. H. Xie of Nanjing Electronic Device Institute is gratefully thanked for the RIE technical assistance. The work is supported by the Chinese National Nature Science Foundation, the Chinese National Basic Science Research Program and National High Technology R&D Foundation.

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