Appl Phys A (2013) 111:719–724
DOI 10.1007/s00339-013-7641-3

Applied Physics A
Materials Science & Processing

RAPID COMMUNICATION

Non-volatile memory effect of a high-density NiSi nano-dots floating gate memory using single triangular-shaped Si nanowire channel

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Received: 12 November 2012 / Accepted: 18 February 2013 / Published online: 26 February 2013
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Abstract A back-gated nonplanar floating gate device based on buried single triangular-shaped Si nanowire channel (width ∼40 nm) and embedded high-density uniform NiSi nano-dots ($\sim 1.5 \times 10^{12}$ cm^{-2}) is demonstrated. Memory properties including memory window, programming/erasing, and retention are evaluated. The transfer and transient characteristics show clear charge injection, storage and removal effects and the associated programming/erasing mechanism based on fringing electric field is studied. Robust room and high temperature retention performance is observed.

1 Introduction

The invention of Si nano-dot floating gate memory has stimulated broad interests among nonvolatile memory community thanks to the improved reliability, CMOS compatible process, and its promise of scalability when the golden era of flash technology is approaching the limit [1]. Nano-floating gate memory employing different types of nano-dots, namely, semiconductor [2, 3], metal [4, 5], metallic silicide [6–8], core-shell dots [9, 10], and dielectrics [11, 12], have received extensive investigation. Moreover, energy band structure engineering has been widely carried out adopting varied dielectric stack [13–16] in order to enhance the memory performance for scaled technology nodes. Nevertheless, problems of this technology have inevitably arisen as device dimensions are reduced. Despite all the efforts spent, dot density fluctuation among others remains the most serious issue in miniaturized cells [17, 18]. In light of these problems, a floating gate layer with high density nano-dots of superior uniformity becomes an essence. In addition, increasing the number of dots per cell by nonplanar channel architectures can be another possible solution due to increased cell area.

Toward the goal of nonplanar devices, efforts have been put into exploring various channel structures, among which the most attractive ones are FinFETs [19] and surrounding-gate vertical FETs [20]. With their nanocrystal memory variants also proposed and developed [21–23], these nonplanar technologies have well extended logic and memory transistor dimensions to the third one. An alternative approach to realize nonplanar device channel is to adopt nanowires (NWs), which have been nominated building blocks for future electronics for their unique electronic properties and scalable dimensions. Nano-floating gate memory devices employing NW channel have been reported, aiming at maximizing both the charge storage and transport capabilities [24, 25]. However, the nano-dots used in these studies were randomly spin-coated colloidal dots with low sheet density, leaving limited control over the size and density distribution of the nano-dots. The size of NW was also relatively large, around 90–120 nm. Hence, it is desirable to develop more favorable methods for nano-dots synthesis to promote the advantages brought by nonplanar channel, particularly when the channel size is reduced to deep-scaled regime. Recently, we have reported a memory device based on the multi-Si NW channel [26]. This device combines the nonplanar cell with high-density uniform metallic silicide NC

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as charge storage nodes, providing a possible way to extend the scaling limit of NC memory devices.

In this paper, we report an ultrascaled nonplanar NiSi NC memory device with single triangular-shaped SiNW channel enclosed by one Si (100) plane and two Si (111) planes on a SOI substrate. Although similar NW fabrication process was employed as in [26], single NW channel rather than multi-NW channel would reduce the complexity of each cell for reliable device performance and also significantly increase data storage density in future memory array integration. Furthermore, dot density variation is an effect directly associated with device dimensions and becomes more and more evident as the cell size shrinks. Therefore, it is necessary to realize a device with scaled dimensions by this nonplanar technology for further clarification and future applications. In contrast to the large size of the earlier demonstrated multi-Si NW channel [26], the size (base) of the NW employed in this work is aggressively scaled to around 40 nm. This physical size could be adopted in 22 nm technology node if similar design rule demonstrated in 90 nm technology node NC memory array could be used [27]. Since the angle between Si (100) and (111) planes is 54.74°, compared to planar device with the same floor area, the number of NCs that controls cell states is almost doubled in this nonplanar device, leading to less dot density variation problems and enhanced cell operation reliability.

2 Device fabrication

Figure 1 shows the schematic of the structure of the back-gated device and its step-by-step fabrication process flow. First, phosphorus ion implantation was performed on a commercially available SOI wafer (Soitec, inc.) with 88 nm p-type Si (100) active layer and 145 nm buried oxide layer to achieve a doping concentration of 10^{18} cm^{-3}. Then dopants were activated using rapid thermal annealing (RTA) at 950 °C for 60 sec. Stand-alone Si NWs were obtained on buried oxide surface via top-down wet chemical etching by the KOH solution. After a DI water rinse, a 5 nm thermal oxide was formed by dry oxidation on the surface of NWs as the tunneling layer. High-density NiSi nano-dots were deposited over the whole sample surface as floating gate for charge storage by vapor-solid-solid (VSS) method. VSS has been a traditional way used for NW growth study [28]. However, the initial stage of the VSS growth to form silicide nano-dots before the formation of NWs can be a reliable and reproducible way for high-density storage nodes preparation as reported in our previous work [8, 15]. To perform VSS growth, a very thin layer of Ni was deposited by e-beam evaporation on the sample surface, followed by immediate transfer of the sample into low pressure chemical vapor deposition system for NiSi nano-dots growth at 575 °C using SiH_4 as Si precursor. 40 nm Al_2O_3 was deposited by atomic layer deposition to cover the nano-dots/NW surface as passivation. Schematics (f) through (g) in Fig. 1 show the view of the subsequent fabrication steps from the cutting plane AA′. By using E-beam lithography, two electrode patterns were aligned onto the SiNW to create two openings for the next etching step. After removing Al_2O_3/nano-dots/SiO_2 layers by wet etching using diluted HF (1:100) for 30 sec, SiNW was exposed in the opened windows. Ti/Au was deposited by room temperature E-beam evaporation as direct metal contacts to the SiNW and the two electrodes were formed by a lift-off process. Previously junction-less transistor was reported as being advantageous in terms of the simplified fabrication process and promise of scalability [29]. The benefit of this type of device can be more pronounced in scaled devices where source/drain implantation becomes extremely challenging. Here, we adopt this junction-less structure for our memory with a NW channel in line with the scaling requirements of nano-floating gate memory device. Aluminum was also deposited to the back side of the wafer to make good back gate contact. A control device with no nano-dots embedded was fabricated simultaneously for comparison.

3 Results and discussion

The device at different stages of the fabrication process flow was characterized by scanning electron microscopy (SEM) and transmission electron microscopy (TEM). Figure 2(a) shows an SEM image of the triangular shaped SiNW on buried oxide at a tilted angle. SEM images in Fig. 2(b) show the top view of nano-dots distributed on top of a NW and at the open area of the sample right after VSS growth. As shown in the inset image, a nano-dots layer with high density of 1.5×10^{12} cm^{-2} is achieved with ultra-uniform distribution and average size of 4.5 nm. The high-resolution X-ray photoelectron spectroscopy (XPS) data obtained from the nano-dot layer for Ni $2P_{3/2}$ in the inset of Fig. 2(b) shows a binding energy at 853.9 eV, confirming that the nature of NCs is NiSi [30]. Figure 2(c) shows a cross-sectional TEM image of the device after Al_2O_3 coverage. The TEM sample was prepared by Focus Ion Beam (FIB) and an embedded layer of nano-dots can be clearly seen. Figure 2(d) shows a SEM image of the finalized device with two metal electrodes.

The current-voltage characteristics of this memory device were tested by an Agilent 4155C semiconductor analyzer. Clear memory effect is shown in the transfer characteristics of the device at neutral, programmed and erased states in Fig. 3. As seen from the figure, the phosphorus doped NW device shows enhancement mode n-type characteristics and the current level in this device is very low. This is due to the Schottky contacts formed between the metal electrodes

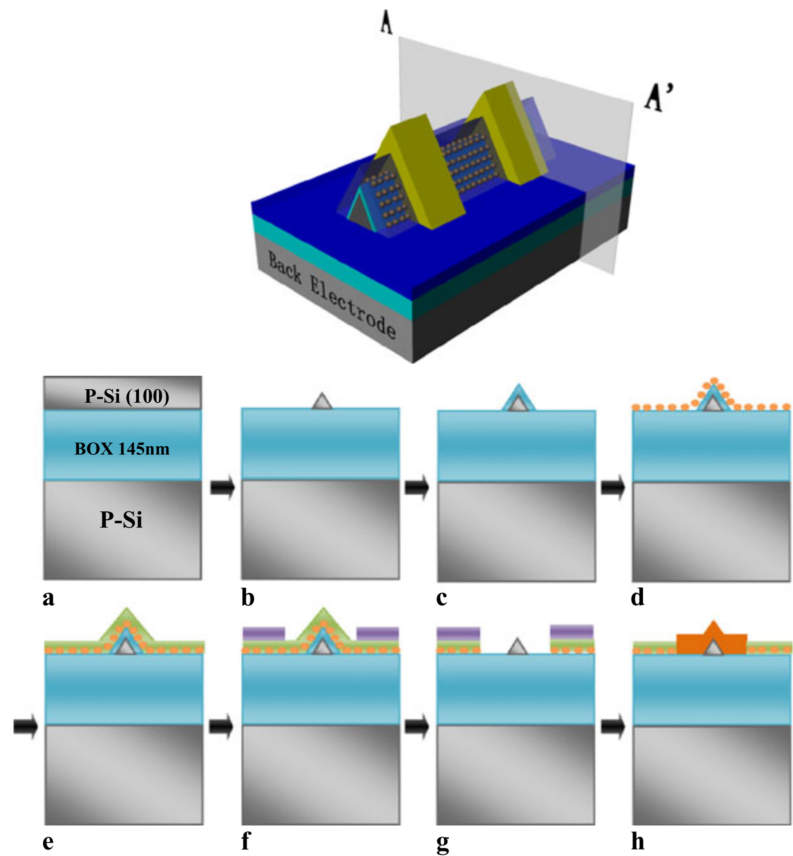

Fig. 1 Schematic of back-gated device structure and fabrication process flow: (**a**) SOI wafer; (**b**) SiNW after etching; (**c**) tunneling oxide by dry oxidation; (**d**) nano-dots deposition; (**e**) Al_2O_3 passivation; (**f**) E-beam lithography patterning of S/D; (**g**) wet etching to expose SiNW channel; (**h**) contact metal deposition

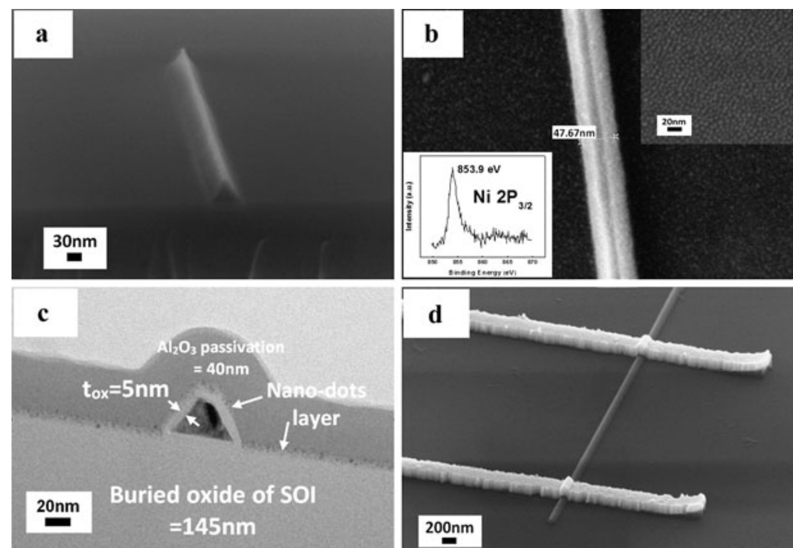

Fig. 2 (**a**) Tilted cross-sectional SEM view of stand-alone triangular-shaped SiNW (~40 nm); (**b**) top view SEM image of high-density nano-dots on tunneling oxide-covered SiNW; *inset*: SEM image of evenly distributed nano-dots at open area (1.5×10^{12} cm^{-2}) and XPS result of the nano-dots layer; (**c**) cross-sectional TEM image of triangular SiNW embedded in Al_2O_3; (**d**) SEM image of source/drain contacts of as-fabricated device by E-beam lithography

and SiNW, which leads to on-state currents at nano-ampere scale. Contact resistance plays a significant role in determining the current-voltage properties of NW devices where device features shrink to nanometer scale and good ohmic contact formation becomes extremely challenging [31, 32]. Despite of the low current level, the memory effect of this device is the focus and of more concern in this work. Source and drain are grounded during programming/erasing. When a pulse of 60 V/1 sec is applied to the back gate, the I_d–V_g curve shows a large shift to the right, suggesting the charging of the floating gate (nano-dots) and the shift of threshold voltage (ΔV_{th}) is due to the excess electric field imposed by the stored charges. In contrast, when the device is erased by a negative pulse of −60 V/1 sec, the charges in the floating gate are pulled back to the channel and the curve shifts back to the left. The control device exhibits negligible shift

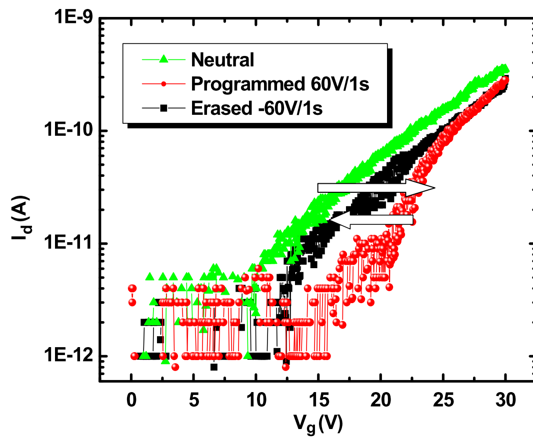

Fig. 3 Transfer characteristics of back-gated nonplanar nano-floating gate memory at neutral, programmed and erased states

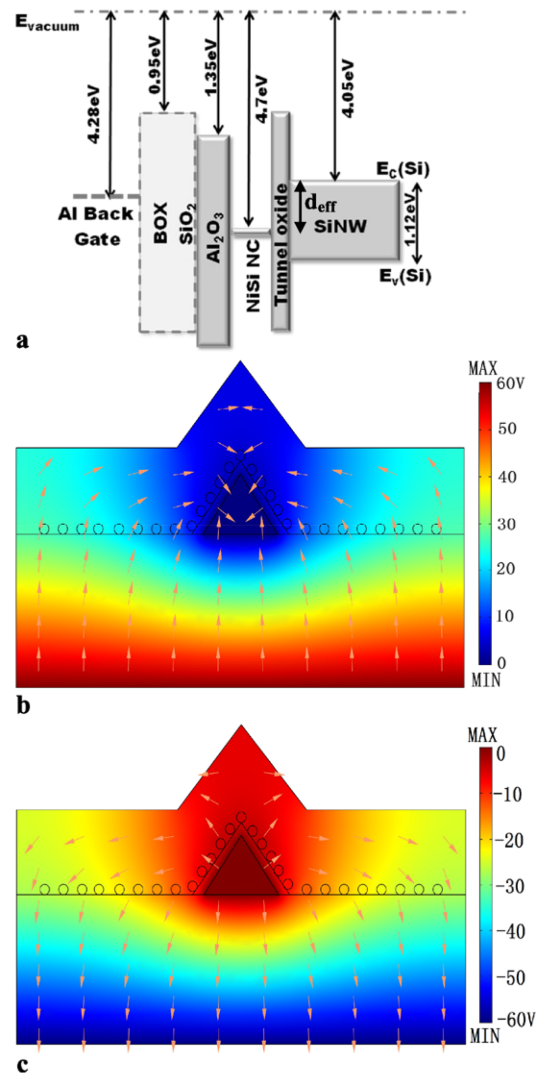

Fig. 4 (**a**) Equivalent energy band diagram of back-gated nonplanar nano-floating gate memory, work function of NiSi ∼ 4.7 eV; (**b**) fringing electric field direction during programming; (**c**) fringing electric field direction during erasing

in I_d–V_g curves under the same operation conditions (not shown here), which also confirms that the memory effect stems from nano-dots charging/discharging rather than defect/trap charge storage. The high gate voltage required to bias the back gate is due to the existence of thick buried oxide layer in the wafer and the inefficiency of fringing field programming/erasing mechanism.

Due to particular geometries of the back gate and channel, this NW device relies on fringing electric field originating from the back electrode to implement the programming/erasing processes [33, 34]. Figure 4(a) shows the equivalent energy band diagram of the device. The gate and buried oxide layer are in dashed line because in real device they should be on the back side of SiNW. During programming/erasing operations, the buried oxide layer serves as part of control oxide while in retention state charges are kept in the deep quantum well formed by Al_2O_3/NiSi nano-dots/tunneling SiO_2 sandwich structure thanks to the large conduction band offset and work function of NiSi. Simulation results in Fig. 4(b) and (c) from Comsol Multiphysics qualitatively show the direction of electric field within the device around the channel at programming and erasing states, respectively. In contrast to the one-dimensional SiNW channel, the whole back side of the sample acts as the back electrode and the area of this back gate is so large that it can be considered two-dimensional. During programming process, the channel is grounded and a positive bias is pulsed on the back gate. In this case, the electrical potential of the nano-dots layer is lower than that of the back gate but higher than that of the channel, and the electric field starting from the back electrode is oriented from the nano-dots toward the channel. This field accounts for the charging of nano-dots and the right shift of the I_d–V_g curve under a positive bias. Similarly, the back gate is negative biased when the device is erased (Fig. 4(c)) and electrons are pulled from the nano-dots back to the channel due to the fringing field and capacitive coupling among gate, nano-dots and NW channel. Therefore, when a negative pulse is applied, the I_d–V_g curve shifts to the left to erased state.

The programming/erasing behavior of this device was studied via testing the transient performance and examining ΔV_{th} under varied back gate bias. Threshold voltages (V_{th}) of the device at different states are extracted by I_d–V_g curve sweeping and linear extrapolation of the curve at the point of maximum slope to x-axis where $I_d = 0$ [35]. As shown in Fig. 5(a), for each gate voltage, ΔV_{th} increases with programming/erasing time until saturation starts to occur at millisecond scale. Under gate voltage of ±50 V, the device exhibits ΔV_{th} of 3.2 V and 1.8 V at around 30 ms for programming and erasing, respectively. With a higher gate bias of ±80 V, larger ΔV_{th} of 12 V and 10.3 V is observed under the same writing/erasing time.

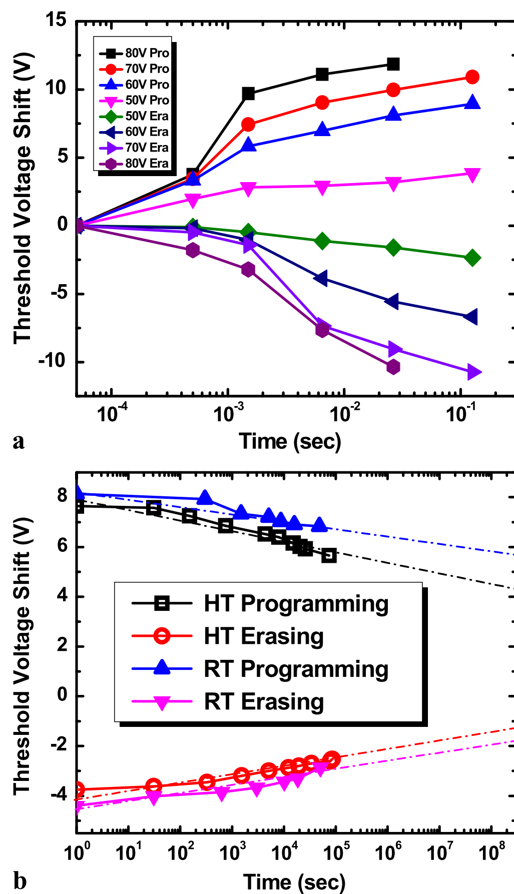

Fig. 5 (**a**) Programming/erasing characteristics of back-gated nonplanar nano-floating gate memory under varied gate bias; (**b**) room-temperature and high-temperature retention properties of back-gated non-planar nano-floating gate memory

Threshold voltage shift caused by one electron storage in each nano-dot (ΔV_{th0}) can be estimated by rough calculation as follows: $Q_0 = De = 1.5 \times 10^{12}\ \text{cm}^{-2} \times 1.6 \times 10^{-19}\ \text{C} = 2.4 \times 10^{-7}\ \text{C/cm}^2$, where Q_0 is the charge sheet density assuming each nano-dot is charged evenly by one electron, D is the sheet density of nano-dots and e is the unit charge. Then $\Delta V_{th0} = Q_0/C_{\text{control}} \sim 10$ V is the resulted threshold voltage shift with this device geometry, with C_{control} being the equivalent control oxide capacitance (consider $t_{\text{BOX}} = 145$ nm, assume a control oxide thickness of 150 nm). From the programming/erasing behavior shown by Fig. 5(a), we observe a saturation of ΔV_{th} at around 10 V for the gate bias used, which indicates that on average only one electron is injected into each nano-dot. The poor efficiency of fringing-field writing/erasing scheme and the thick buried oxide are responsible for this small shift.

Charge retention characteristics of the device were also obtained at both room temperature and high temperature of 85 °C, as shown in Fig. 5(b). The device at neutral state was first programmed/erased at ±60 V/1 sec for electron/hole injection to the nano-dots and ΔV_{th} was tracked and recorded as a function of waiting time to determine the loss of stored charge. In the beginning right after charge injection, the opening between two states, namely, programmed and erased, is around 12 V. After around 10^5 sec, slight shrinkage happens and the opening decreases to 10 V for room temperature case and 8.5 V for high temperature case. As far as typical flash memory retention time of 10 years is concerned, extrapolated lines of ΔV_{th} change suggest an linear trend with more than 50 % of the charge remained and a clear separation of the two states for both room temperature and high temperature case. The good high-temperature retention performance of this device can be attributed to the robust thermal stability of NiSi nano-dots as reported in previous work [15]. Another possible contributing factor is the elevated energy levels in small NW channel that makes it harder for stored charge to tunnel back from nano-dots [36].

4 Conclusion

A combination of high-density NiSi nano-dots and scaled single SiNW is used to implement a non-planar nano-floating gate memory. The nano-dots layer with excellent size and location distribution provides a viable way to minimizing dot density variation effect while the non-planar nature of triangular-shaped Si NW channel allows for more dots within single cell to further mitigate the issue in scaled devices. This back-gated device relies on fringing electric field to fulfill memory operations, i.e., programming and erasing, and shows good room-temperature and high-temperature retention performance. This research suggests that NC memory technology can be potentially scaled into 22 nm technology node by using nonplanar device geometry.

Acknowledgements This material is based on research sponsored by DARPA/Defense Microelectronics Activity (DMEA) under agreement number H94003-10-2-1003 and the National Science Foundation (NSF) DMR-0807232.

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