P-type behavior of Sb doped ZnO from p-n-p memory structure

Jian Huang, Zonglin Li, Sheng Chu, and Jianlin Liu[a)]
Quantum Structures Laboratory, Department of Electrical Engineering, University of California, Riverside, California 92521, USA

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Antimony (Sb) doped p-type ZnO was studied by using Sb-ZnO/ZnO/Sb-ZnO p-n-p structure. Secondary ion mass spectrometry result confirmed the formation of the structure. Rectifying current-voltage characteristics between Sb-ZnO and undoped ZnO layers were achieved, proving the p-n junction was formed. The p-type behavior from the p-n-p structure was studied by using the capacitance-voltage measurement and small signal model. The voltage operation led to the charging/discharging of the structure, showing nonvolatile memory effect. Very long retention time was achieved. This research suggests that p-type ZnO can be evaluated by a p-n-p structure, which could be promising for future nonvolatile memory applications. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4769097]

ZnO, as a II-VI wide band gap material, has attracted significant attention in the last few years.[1–3] However, due to the "intrinsic" donors such as zinc interstitials and oxygen vacancies[4,5] and the unintentional donor hydrogen,[6] reliable p-type conductivity is difficult to achieve, which poses the largest obstacle on the application of ZnO. The group V elements are considered to be p-type dopants for ZnO, and a great deal of efforts has been made to achieve the p-type conductivity.[7–9] Based on first-principle calculations, antimony (Sb) can produce shallow acceptor levels in ZnO if Sb atom substitutes Zn atom and connects with two Zn vacancies.[10] Experimentally, our group achieved Sb doped p-type ZnO thin films and nanowires[11,12] and also developed various devices based on Sb doped p-type ZnO such as photodetectors,[3,12] light emitting diodes,[13] and nanowire lasing devices.[14]

While all the p-type ZnO studies at the device level are based on optoelectronic devices and the applications of p-type ZnO are limited within optoelectronic field, the potential of this wide band gap material for nanoelectronic devices such as nonvolatile memory has been largely ignored. On the other hand, demonstration of ZnO nanoelectronic devices based on p-type ZnO materials will also unambiguously prove the p-type conductivities of the materials as their optoelectronic devices had achieved.[12–14] Previously, a memory structure based on wide band gap material was fabricated and characterized using a SiC n-p-n structure.[15] This memory structure can achieve low programming voltage ($\leq$10 V) due to the diode operation mechanism and long retention time (>100 years) due to the low thermal generation current. Compared with SiC, ZnO having a band gap of $\sim$3.2 eV can achieve extremely low thermal generation current, which can further enhance the retention performance of the nonvolatile memory.[15] ZnO is a direct band gap material which has low minority carrier lifetime (nanosecond),[16] and it will result in high programming speed. Furthermore, ZnO can also be synthesized with lower cost using low-temperature epitaxial growth, so it can reduce the cost for future memory devices. In this letter, we report the p-type Sb doped ZnO films based on Sb-ZnO/ZnO/Sb-ZnO p-n-p memory structure. The program and retention performances of this memory structure are also presented.

ZnO p-n-p structure was grown using plasma-assisted molecular-beam epitaxy. First, a thin MgO buffer layer was grown on c-sapphire substrate at 450 °C for 70 s, which was followed by the growth of a ZnO buffer layer at the same substrate temperature for 15 min. Then, an Sb doped p-type ZnO/undoped n-type ZnO homojunction was grown on this MgO/ZnO buffer. The 300 nm thick undoped ZnO film was grown at a substrate temperature of 500 °C with Zn effusion cell temperature of 360 °C. This was followed by the growth of the 300 nm thick Sb doped ZnO layer at a higher substrate temperature of 550 °C with Zn and Sb effusion cells temperature of 360 °C and 390 °C, respectively. In order to activate the Sb dopants, *in situ* thermal annealing was performed in vacuum at 800 °C for 20 min. To form the p-n-p memory device, photolithography and wet etching were used to define the mesa structure. Au/Ni (100/10 nm) were then deposited on p-type ZnO. Lift-off process and proper annealing were used to form Ohmic contact electrodes, and SiO_2 was deposited to passivate the device. Au/Ti (100/10 nm) electrodes were also fabricated on n-type ZnO for one sample, to verify the formation of the p-n junctions.

Figure 1 shows elemental distribution of Zn, O, Sb, and Al in the sample measured by secondary ion mass spectrometry (SIMS). The Al signal is from the sapphire substrate. The sharp stair of Sb distribution between doped and undoped ZnO represents a good interface of the two layers. The atomic percentage of Sb is estimated to be around 1.5%.

Current-voltage (I-V) characteristics were characterized by an Agilent B1500A semiconductor parameter analyzer. Figure 2 shows I-V characteristics of a typical p-n junction after Au/Ni to p-type ZnO and Au/Ti to n-type ZnO contacts were formed (left inset), suggesting typical diode rectifying characteristics. The right inset shows that the Ohmic contacts were formed on both p-type ZnO and n-type ZnO. These results suggest the formation of ZnO p-n junction diodes and thereby p-n-p memory structure.

From Hall effect measurement, the electron concentration, mobility, and resistivity of the undoped ZnO layer are

a)Author to whom correspondence should be addressed. Electronic mail: jianlin@ee.ucr.edu.

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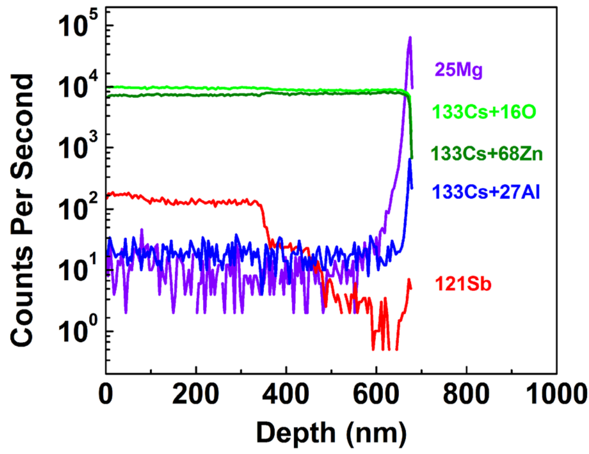

FIG. 1. SIMS result of ZnO p-n junction on c-sapphire substrate. The elemental profiles of Zn, O, Sb, and Al can be seen, which confirm our device structure has been formed.

3.46×10^{17} cm^{-3}, 17.6 cm^2 V^{-1} s^{-1}, and 1.03 Ω cm, respectively. However, it is impossible to extract accurate hole carrier concentration of the top Sb-ZnO thin film of the structure by using Hall effect measurement due to the thick underneath undoped n-type layer. In order to study the p-type behavior of the Sb-ZnO thin film, capacitance-voltage (C-V) characteristics were obtained using a 4284 A LCR meter. Figure 3 shows high-frequency (1 MHz) C-V characteristic of the ZnO p-n-p structure (inset (a) in Fig. 3). The capacitance was measured between the two Au/Ni contacts. The C-V sweep ranges from 0 V to 10 V. As seen from the figure, the capacitance of the device decreases nonlinearly as the applied bias increases.

To quantitatively understand the C-V characteristics and extract hole concentration in the Sb-doped p-type ZnO layer, we can use the small signal model. An equivalent circuit of the p-n-p structure is shown as an inset (b) in Fig. 3. The impedance r_{eq} of this symmetric p-n-p structure can be calculated

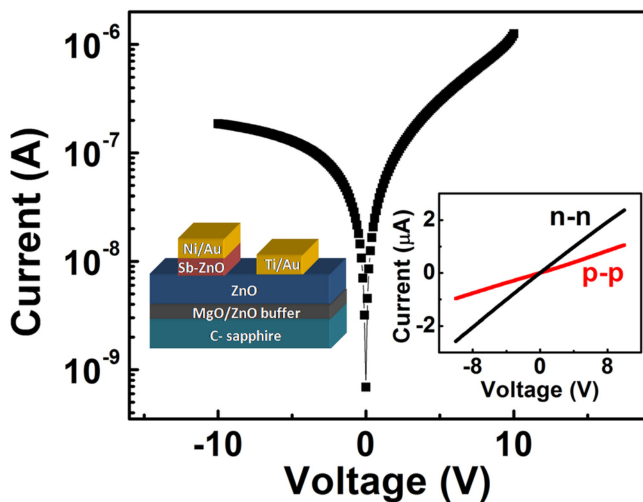

FIG. 2. I-V characteristics of Sb-doped p-type ZnO/undoped n-type ZnO homojunction. Left inset shows the measured device structure. Right inset shows the I-V curves of p-p contacts and n-n contacts, respectively. Ohmic contact behavior is evident.

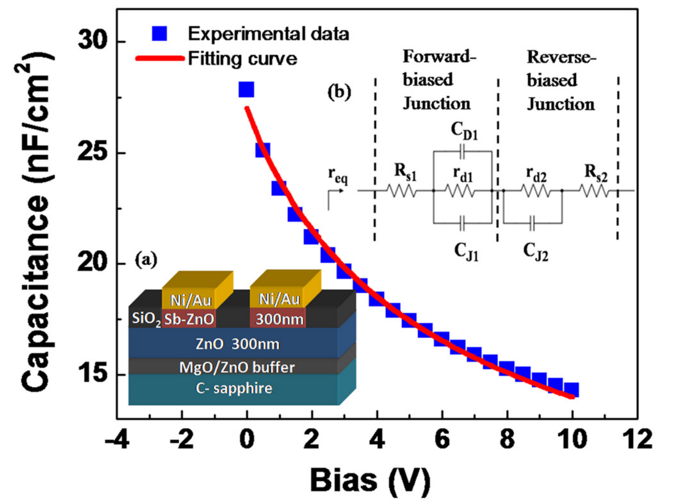

FIG. 3. C-V characteristics of ZnO p-n-p structure on sapphire. The symbols are the experimental data, and the solid line is the fitting result based on small signal model. Inset (a) shows the measured p-n-p memory structure. Inset (b) shows the equivalent circuit of the p-n-p structure.

$$\begin{aligned} r_{eq} &= R_{s1} + r_{d1} \left\| \frac{1}{j\omega C_{D1}} \right\| \frac{1}{j\omega C_{J1}} + r_{d2} \left\| \frac{1}{j\omega C_{J2}} + R_{s2}, \right. \\ &= R_{s1} + \frac{r_{d1}}{j\omega r_{d1}(C_{D1}+C_{J1})+1} + \frac{r_{d2}}{j\omega r_{d2}C_{J2}+1} + R_{s2}, \\ &= R_{s1} + R_{s2} + \frac{1}{\omega^2 r_{d1}(C_{D1}+C_{J1})^2} + \frac{1}{j\omega \dfrac{(C_{D1}+C_{J1})C_{J2}}{C_{D1}+C_{J1}+C_{J2}}}, \end{aligned} \tag{1}$$

where the imaginary part $j\omega \frac{(C_{D1}+C_{J1})C_{J2}}{C_{D1}+C_{J1}+C_{J2}}$ clearly shows that the total capacitance can be viewed as $C_{D1}+C_{J1}$ in series with C_{J2}.The reverse-biased junction capacitance C_{J2} can be calculated by

$$C_{J2} = \frac{\varepsilon A}{x_n + x_p} = \frac{\varepsilon A}{\sqrt{\frac{2\varepsilon(V_{bi}+V_A)}{q(N_A+N_D)}}\left(\sqrt{\frac{N_A}{N_D}} + \sqrt{\frac{N_D}{N_A}}\right)}. \tag{2}$$

Here, ε is dielectric constant, A is area, q is electron charge, V_{bi} is the built-in potential of the p-n junction, x_n and x_p are the depletion region thicknesses in n-type and p-type ZnO, respectively, and N_A and N_D are acceptor and donor concentration, respectively. Because the reverse-biased junction and forward-biased junction are in series, the voltage drop across the forward-biased junction only shares a very small portion of the applied bias. Thus, the diffusion capacitance C_{D1} can be ignored, and the junction capacitance of a forward-biased junction is calculated by $C_{J1} = A\sqrt{\frac{8\varepsilon q N_A N_D}{V_{bi}(N_A+N_D)}}$. So for the p-n-p structure, the total capacitance is

$$C(V_g) = \frac{C_{J1} \times C_{J2}(V_g)}{C_{J1} + C_{J2}(V_g)}. \tag{3}$$

From the fitting by using Eq. (3) (the solid line in Fig. 3) and the electron concentration of 3.46×10^{17} cm^{-3}, $N_A = 5.95 \times 10^{16}$ cm^{-3}, and $V_{bi} =$ 2.71 V are obtained.

The decrease of the capacitance at higher voltage also suggests that this p-n-p structure can act as a charge storage device. When a bias is applied on the p-n-p structure, one p-n junction is forward-biased while the other one is reverse-biased. The electrons inside the n-layer flow out of the structure from the forward-biased junction, while the n-layer also receives small amount of electrons from the reverse-biased junction until the potential of the n-layer cannot increase further under this applied voltage. The net effect is the built-up of positive space charges inside the n-type layer, or charging the n-layer. In the mean time, the width of the space charge region of the reverse-biased p-n junction increases.

To evaluate the charging, or programming operation, an Agilent 81104 A pulse generator was used to operate the device, and the capacitance was read from an Agilent 4284 A LCR meter at 0 V. In this situation, after the bias is removed, the programmed extra space charges in the n-layer will redistribute and reverse both p-n junctions. The space charge region width of both junctions is larger, and thus the capacitance is smaller than that of the junctions before programming. Figure 4(a) shows capacitance change (ΔC) as a function of different program pulse height. The pulse width was fixed at 1 s. Under the program pulse larger than 2 V, the absolute value of ΔC increases as the pulse height increases, which indicates that more charges are developed inside the structure under higher pulse. Figure 4(b) shows ΔC for different pulse width. The pulse height was fixed at 10 V, and the pulse width was changed from 1 μs to 1 s. The absolute value of ΔC begins to increase after the pulse width is larger than 10 μs and reaches saturation at 0.1 s. This programming speed is slow but reasonable considering the low voltage operation.

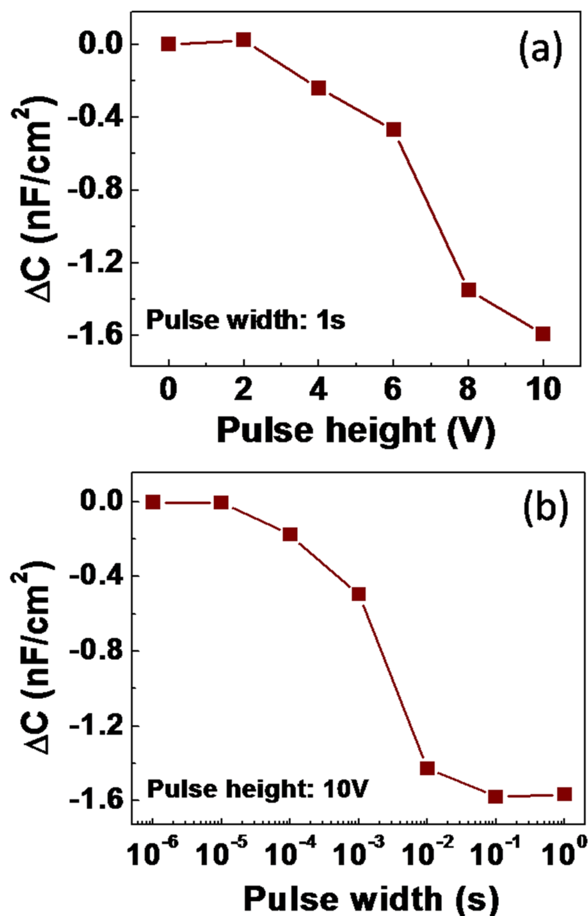

FIG. 4. Programming performance of ZnO p-n-p memory structure. ΔC is the change of the capacitance before and after programming. All the capacitance is read at 0 V bias. (a) Using programming pulses with different pulse height and 1 s pulse width. (b) Using programming pulses with different pulse width and 10 V pulse height.

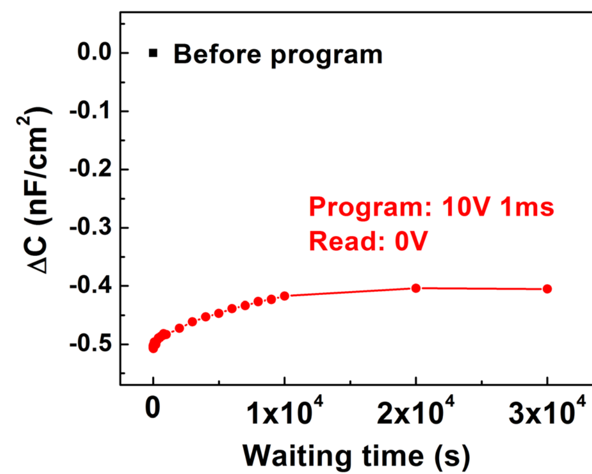

FIG. 5. Retention characteristics of ZnO p-n-p memory structure programmed at 10 V for 1 ms.

Figure 5 shows retention characteristics of the ZnO p-n-p structure. The device was programmed with 10 V for 1 ms, and the capacitance measured at 0 V was plotted as a function of the waiting time. After the programming, excess space charges are developed and reverse-bias both p-n junctions. The reverse-biased p-n junctions have net generation rate, and the carriers from thermal generation will neutralize the excess space charges until both junctions return to equilibrium. As the thermal generation rate is exponential to the reciprocal of the band gap energy, it will take extremely long time for a defect free device to return to thermal equilibrium. However, the defects are unavoidable in the ZnO, and these defects will help the generation process and thus neutralize some excess space charges. As seen from the figure, during the early stage, the capacitance increases about 20% of the total ΔC after programming. This shall be due to the thermal generation of both bulk Shockley-Read-Hall defect levels and other levels originated from surface states. After 10^4 s, the capacitance remains almost constant, which indicates the amount of the charges trapped inside the structure become stable. This result suggests that the defects in the present material do not significantly discharge the device and this ZnO p-n-p structure is capable of achieving much longer retention time than the flash memory, which usually meets 10-year retention standard.

In summary, a ZnO p-n-p structure using Sb doped ZnO as p-type layer and undoped ZnO as n-type layer on c-plane sapphire substrate was fabricated. SIMS result showed good interface between Sb doped and undoped layers. The formation of p-n junction was proved by the good rectification behavior between p-type layer and n-type layer by I-V measurements. A hole concentration $N_A = 5.95 \times 10^{16}\ \mathrm{cm}^{-3}$ was obtained from the fitting of the C-V curve by using small signal model, which cannot be done by Hall effect measurement. The nonvolatile memory effect of the p-n-p structure related to the charge storage in the n-layer of the p-n-p structure was

also studied. The program and retention characteristics showed that ZnO p-n-p memory structure can achieve low operation voltage and long retention time, which suggests that the Sb doped p-type ZnO could be excellent material for future memory application.

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