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Rapid thermal oxygen annealing formation of nickel silicide nanocrystals for nonvolatile memory

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Abstract Discrete NiSi nanocrystals were synthesized by rapid thermal oxygen annealing of very thin Si/Ni/Si films on a SiO_2 tunneling layer. They were used to fabricate metal–oxide–semiconductor capacitor memory. Electrical properties of the memory device such as programming, erasing and retention were characterized and good performance was achieved.

1 Introduction

A great deal of current research is focused on seeking a solution for the continued scaling of nonvolatile memory [1, 2]. Nanocrystal (NC)-based memory devices have been extensively studied since they were discovered by Tiwari et al. [3]. Memories based on NCs synthesized by different ways, such as chemical/physical vapor deposition (CVD/PVD) [4–6], vapor solid solid (VSS) growth [7], evaporation [8] and organic synthesis [9] were fabricated in order to improve the device performance. Furthermore, new types of NC floating dots, such as Ge NCs [10], metal [11–14] or metal-like [15] dots and dielectric NCs (Al_2O_3, HfO_2, Si_3N_4, etc.) [16–18], were used to achieve memory devices with prolonged retention performance. Among these materials, silicide was recognized as a good candidate for a floating gate due to its high thermal stability and large work function [19]. Silicide NCs have been synthesized by using reaction of metal and Si NCs [19] and VSS methods [7]. As an alternative method, in this work, we carried out in-situ RTO annealing of a two-dimensional Si/Ni/Si multi-layer structure to form NiSi NCs. Previously, the rapid thermal annealing (RTA) process was already used to form Mo NCs, leading to reasonable memory performance [20]. Compared with other methods, which need longer temperature treatment processes, RTO and RTA processes use a short high temperature process to reduce the detrimental effect on other parts of the devices to preserve high memory performance.

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2 Device fabrication and characterization

The process started on a p-type Si substrate. The RTO annealing process of fabricating NiSi NCs began with a 5-nm thermal oxide formation at 850 °C after a standard pre-furnace clean process. Si, Ni and Si thin films of 2 nm each were grown sequentially in a Temescal electron beam evaporation system. The system was under a vacuum of 1×10^{-6} Torr and the substrate temperature was room temperature. The growth rate for each layer was 0.1 Å/s. After the sample was removed from the electron beam evaporator, an annealing procedure was performed in oxygen at 650 °C for 30 s to form NiSi NCs. A FEI transmission electron microscope (TEM) with an acceleration voltage of 200–300 kV, a Veeco Dimension 5000 atomic force microscope (AFM) in tapping mode and a PHI 5400 X-ray photoelectron spectroscope (XPS) were used to characterize the morphology and chemical nature of the NCs. The sample was then capped with control oxide of about 20 nm in a low-temperature oxide CVD furnace (LTO) at 450 °C using silane and oxygen mixture source gases. The process

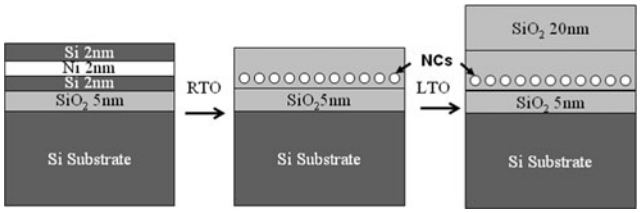

Fig. 1 Process flow for NiSi nanocrystal memory formed by rapid thermal oxidation (RTO)

of in-situ formation of NCs is illustrated in Fig. 1. Top Al electrodes were formed by lithography, electron-beam evaporation of Al and a subsequent lift-off process. A blanket Al layer was also deposited on the back side of the sample to form a bottom electrode. The metal–oxide–semiconductor (MOS) capacitor memory was characterized using an Agilent 4284A LCR meter at room temperature. Typical high-frequency (1 MHz) capacitance–voltage (C–V) sweep operations with a scanning range between ±18 V and ±22 V were used for the device. The sweep started from the inversion to the accumulation, and finally back to the inversion region at a rate of 0.5 V/s.

3 Results and discussion

Figure 2a is a cross-sectional TEM image of NiSi NC memory, showing the morphology of the NiSi nanocrystals which were embedded in the SiO_2 layer. High-resolution TEM (HRTEM) was applied to confirm that these NCs are NiSi. Figure 2b shows a two-dimensional lattice image of one nanocrystal, where the lattice interplanar spacings of 1.92, 1.76, 1.34 and 1.25 Å can be measured from either the image or its fast Fourier transformation, as shown in the small inset. These lattice spacings correspond to the lattice planes of 211, $10\bar{3}$, $31\bar{2}$ and 114, respectively, in orthorhombic NiSi with space group of Pnma (62) and lattice parameters of $a = 5.177$ Å, $b = 3.325$ Å and $c = 5.615$ Å [21]. These lattice planes and their relationships not only indicate that the particle is NiSi, but also enable us to determine the orientation of the nanocrystal relative to the electron beam, that is, the $[\bar{3}7\bar{1}]$ direction of the nanocrystal is parallel to the electron beam. It is difficult to estimate NiSi NC density in the cross-sectional TEM image, so a plan-view TEM specimen was prepared by the focused ion beam (FIB) technique from a memory device with an Al electrode on the top of the NiSi layer and SiO_2 layer. Figure 2c shows a typical plan-view TEM image of NiSi NCs, where, besides NiSi NCs, some Al grain contrast could not be avoided. The density of the NCs was estimated to be at least 1×10^{11} cm^{-2}. Figure 2d shows an AFM image of NiSi NCs after the RTO annealing process. Root-mean-square (RMS) roughness of only 1.5 Å is achieved. The smooth surface of the NC layer allows the

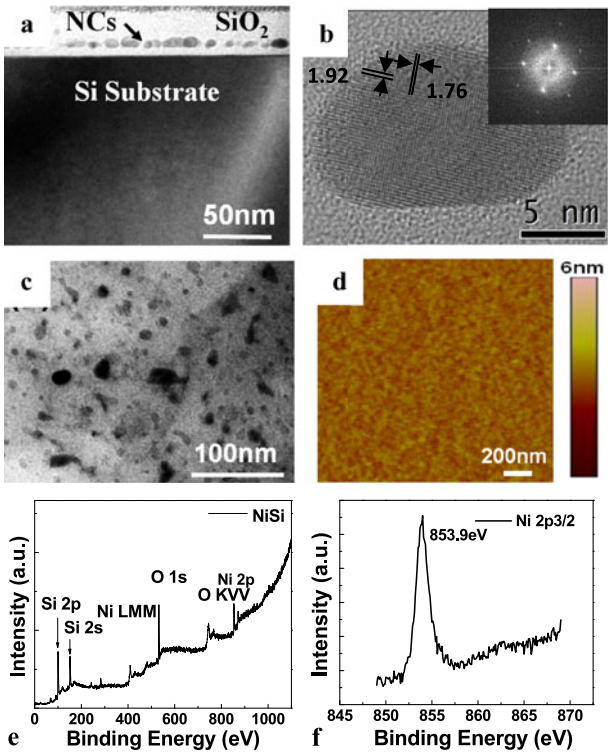

Fig. 2 (**a**) Cross-sectional bright-field TEM image of NiSi NC memory. (**b**) Cross-sectional high-resolution TEM image of one NiSi NC and its fast Fourier transformation (*inset*). (**c**) Plan-view TEM image of NiSi NCs. (**d**) AFM image of NiSi NC layer. (**e**) XPS survey spectrum of NiSi NCs on SiO_2/Si substrate. (**f**) High-resolution scan of the Ni 2p peak

subsequent control oxide layer to be smooth across the cell area, which cannot be done in other NC formation processes. An XPS survey spectrum collected from the NCs is shown in Fig. 2e. Figure 2f is the high-resolution spectrum of the Ni 2p level. The peak of Ni 2p3/2 exists at 853.9 eV, which is associated with the stable silicide state of NiSi [22–25]. This is consistent with HRTEM results.

Figure 3 shows C–V sweeping curves for the voltage ranges of −18 to 18, −20 to 20, −22 to 22 and −25 to 25 V. A small memory window of ∼0.4 V is shown at ±18 V sweeping. As the sweeping voltage increases, hysteresis becomes evident. When the sweeping voltage range increases to 20, 22 and 25 V, the memory window increases to 1.6, 3 and 5.6 V, respectively. A wider voltage sweeping range leads to more electrons to be programmed into the NCs and erased from the NCs by Fowler–Nordheim (F–N) tunneling, and therefore results in a larger memory window.

Figure 4 shows the flat band voltage shift (ΔV_{FB}) as a function of writing time and erasing time. When charges are stored in the floating gate, the electric field is screened by the charges, which results in the flat band voltage shift. It is evident that ΔV_{FB} increases with the increase of the writing time until it finally saturates. This is due to the fact that as the writing time increases, more and more electrons are injected

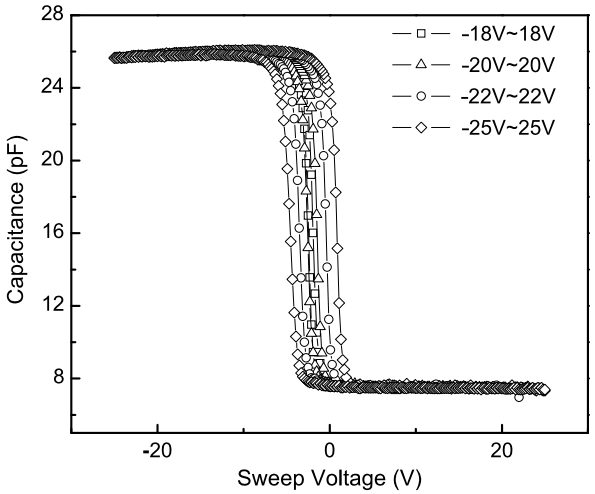

Fig. 3 Typical C–V sweeping curves of MOS capacitor containing NiSi NCs

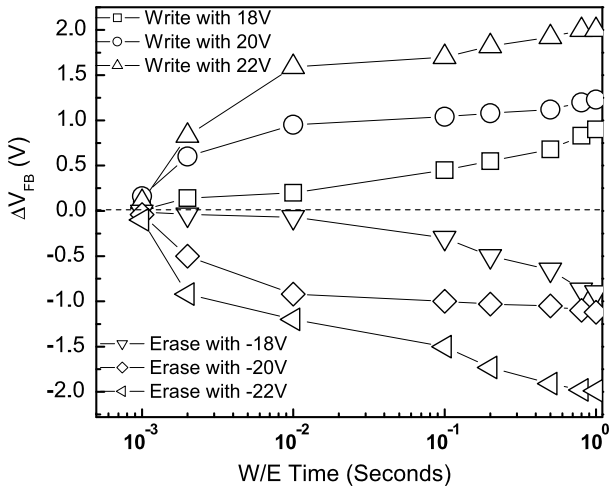

Fig. 4 Flat band voltage shift as a function of writing time and erasing time under different writing and erasing voltages

into the NCs until they are unable to accept more electrons. As the writing voltage increases, ΔV_{FB} also increases fast, which indicates that more electrons go through the tunnel oxide layer by F–N tunneling at higher voltage. Similar to the writing case, ΔV_{FB} increases with the increase of the erasing time, which indicates that more and more electrons are erased from the NCs. In addition, ΔV_{FB} increases with the increase of the erasing voltage, indicating that more electrons go through the oxide layer by F–N tunneling at higher voltage.

Figure 5 shows retention characteristics of NiSi NC memory under programmed and erased states at different temperatures. The device was programmed and erased with gate voltages of ±22 V, respectively, for 100 ms at room temperature and 85 °C. At room temperature, after 10^5 s, the memory window shrinks to 75 % of the original value

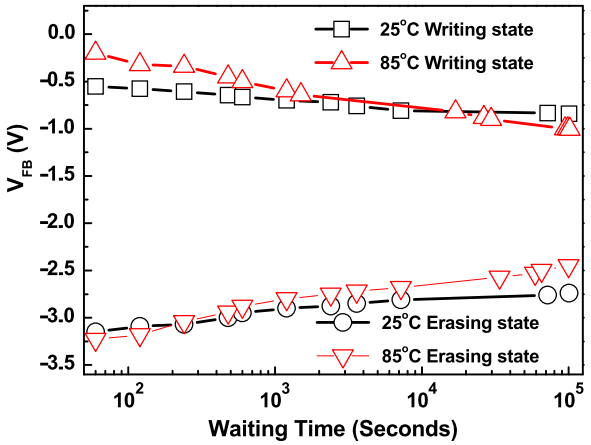

Fig. 5 Retention characteristics of MOS capacitor with NiSi NCs. Data retention time is obtained by monitoring the capacitance at zero gate bias after electron charging at 22 V for 100 ms or hole charging at −22 V for 100 ms, respectively, at both room temperature and 85 °C

and from, extrapolation, 71 % of the electrons would remain after 10 years. At an elevated temperature of 85 °C, the memory window shrinks to 50 % of the original value after the same waiting time of 10^5 s. When the curves are extended to 10 years, the device can still operate without memory window close up.

4 Conclusion

NiSi NCs were synthesized by a RTO process. MOS capacitor memory with NiSi NCs as the floating gate was fabricated and characterized. Good programming, erasing and retention performances were demonstrated. The RTO fabrication process to synthesize NiSi NCs is easy to be implemented, which is promising for future nonvolatile memory technologies.

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