Programmable On-Chip ESD Protection Using Nanocrystal Dots Mechanism and Structures

Zitao Shi, Xin Wang, Jian Liu, Lin Lin, Hui Zhao, Qiang Fang, Li Wang, Chen Zhang, Siqiang Fan, He Tang, Bei Li, Albert Wang, *Fellow, IEEE*, Jianlin Liu, and Yuhua Cheng, *Fellow, IEEE*

***Abstract*—This paper reports a new nanocrystal quantum-dot (NC-QD)-based tunable on-chip electrostatic discharge (ESD) protection mechanism and structures. Experiments validated the programmable ESD protection concept. Prototype structures achieved an adjustable ESD triggering voltage range of 2.5 V, very fast response to ESD transients of rising time $t_r \sim 100$ ps and pulse duration $t_d \sim$ ns, ESD protection density of 25 mA/μm in human body model and 400 mA/μm in charged device model equivalent stressing, and a very low leakage current of $I_{\rm leak} \sim 15$ pA. The NC-QD ESD protection concept can potentially be used to design field-programmable on-chip ESD protection circuitry for mixed-signal ICs in nanoscales.**

***Index Terms*—Electrostatic discharge (ESD), ESD protection, nanocrystal quantum dot (NC-QD), tunable.**

I. Introduction

ELECTROSTATIC discharge (ESD) failure is a major reliability problem to ICs and on-chip ESD protection is mandatory to all ICs and electronic systems [1]–[3]. Accurate ESD protection design must include ESD-critical parameters, e.g., ESD triggering voltage and current (V_{t1}, I_{t1}), holding voltage and current (V_h, I_h), discharging resistance ($R_{\rm ON}$), failure voltage and current (V_{t2}, I_{t2}), etc. As depicted in Fig. 1, practical on-chip ESD protection design for complex mixed-signal ICs must follow the ESD design window that is defined by supplies $V_{\rm DD}$, breakdown voltage BV, and total supply current $I_{\rm DD}$. All ESD-critical parameters must meet the ESD design window to ensure whole-chip ESD protection without latch-up [4]. As IC technology scaling continues, the ESD design window shrinking becomes an emerging ESD design challenge [4]. First, complex mixed-signal ICs using multiple supplies requires flexible ESD V_{t1} across the chip, which disqualifies most traditional ESD protection structures. Second, emerging nanoscale devices and circuits require new nano-ESD protection solutions. Hence, as IC technology migrates into nanoregimes and IC complexity continues increase, novel ESD protection with adjustable ESD triggering V_{t1} is highly desired for mixed-signal ICs to allow local ESD protection design optimization on a chip. This paper reports the first new nanocrystal quantum dot (NC-QD) ESD protection concept, operation mechanism, and prototype designs to address the new ESD design window design challenge.

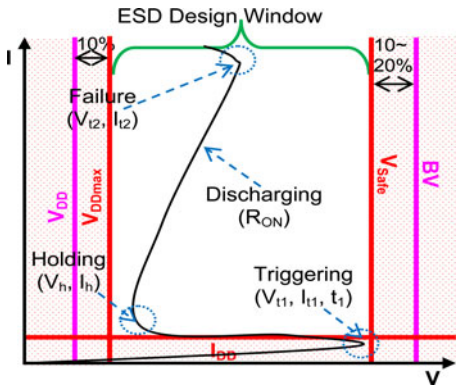

Fig. 1. ESD design window sets the design matrix to ensure whole-chip ESD protection while avoiding possible latch-up effect. A varying safety margin may be required in practical IC designs.

II. NC-QD ESD Protection Structure

Nanocrystal dot-based memories have been studied recently, which utilize a layer of programmable nanocrystal dots to realize bistate memory function [5]–[10]. Benefited from this memory mechanism, we devised the first NC-QD-based programmable NC-QD ESD protection concept and fabricated NC-QD ESD protection structures in a COMS-compatible process. Fig. 2 describes the new silicide-coated NC-QD ESD protection structure and its energy band diagrams. In principle, an NC-QD ESD protection structure is an MOSFET with nanocrystal dot arrays in the floating gate layer, which is connected as an ESD protection unit. For example, an NC-QD grounded-gate NMOSFET ESD protection structure (ggNMOS) can be formed by shortening the gate, source, and body well terminals, which is then connected to the I/O pad and supply bus on a chip [1]. In addition, the new NC-QD ESD structure can also be connected as a gate-coupled NMOSFET (gcNMOS) or a power clamp subcircuit for on-chip ESD protection [3].

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Z. Shi, H. Zhao, L. Wang, C. Zhang, B. Li, A. Wang, and J. L. Liu are with Department of Electrical Engineering, University of California, Riverside, CA 92521 USA (e-mail: aw@ee.ucr.edu).

X. Wang and S. Fan are with Fairchild Semiconductor Corporation, Irvine, CA 92618 USA.

J. Liu is with RF Micro Devices, Greensboro, NC 27409 USA.

L. Lin is with IBM, Microelectronics, Essex Junction, VT 05452 USA.

Q. Fang is with Broadcom Corporation, Irvine, CA 92617 USA.

H. Tang is with OmniVision Technologies, Santa Clara, CA 95054 USA.

Y. Cheng is with Shanghai Research Institute of Microelectronics, Peking University, Shanghai 201203, China.

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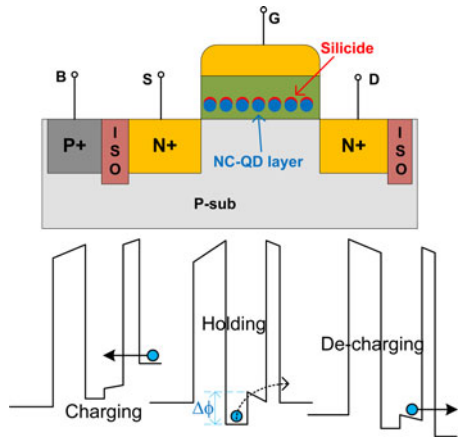

Fig. 2. New NC-QD ESD protection mechanism utilizes the tunneling-assist ESD triggering concept to program the ESD V_{t1}. *Upper*: cross section for the NC-QD ESD protection structure. *Lower*: NC–QD energy band diagrams explaining the charging/decharging mechanisms for the NC–QD ESD protection structures.

The charging/decharging concept is used to program the nanocrystal dot layer of the NC-QD ESD protection structure to adjust its ESD triggering voltage V_{t1} as needed. The traditional ggNMOS ESD protection structure relies on the drain breakdown to trigger ESD discharging under ESD stressing, where V_{t1} is mainly determined by BV_D of the MOSFET that is fixed by the MOSFET doping profiles. Our new tunable-V_{t1} NC-QD ESD protection structure utilizes two new possible tunneling-assist ESD triggering mechanisms: first, the programming of the nanocrystal dots can change the MOSFET threshold voltage V_{th}, which, in turn, will alter the ESD V_{t1}. Second, varying the gate bias V_G by design can change the maximum electric field $E_{\max}$ inside the gate oxide and channel, thus altering $\mathrm{BV}_{\mathrm{DS}}$, which will change the ESD V_{t1}. It can be understood by the following formula:

$$\Delta V_{\mathrm{th}} \approx \frac{q n_{\mathrm{well}}}{\varepsilon_{\mathrm{ox}}} \left(t_{\mathrm{ctl}} + \frac{1}{2} \frac{\varepsilon_{\mathrm{ox}}}{\varepsilon_{\mathrm{Si}}} t_{\mathrm{well}} \right) \tag{1}$$

where t_{well} is the nanocrystal well dimension, n_{well} is the nanocrystal dot density, t_{ctl} is the gate oxide thickness, and ε is the dielectric constant. Several possible on-chip ESD protection schemes may be realized utilizing our new tunable-V_{t1} NC-QD ESD protection structure in practical ESD protection circuit designs, of which, two typical NC-QD ESD protection circuit modes are depicted in Fig. 3. In Scheme-1 shown in Fig. 3(a), the NC-QD ESD protection structure can be connected as a typical ggNMOS ESD protection unit and an external field-programming control (F-program) is connected to the gate, which is used to realize charging/decharging operation through field programming to the control gate. Its ESD protection operation follows the traditional ggNMOS ESD discharging function based upon its parasitic lateral bipolar NPN conduction after ESD triggering and is depicted by the desired snapback *I–V* behavior (see Fig. 1) for efficient ESD discharging. However, its ESD triggering voltage V_{t1} can be readily adjusted by the new NC-QD gate programming mechanism, hence leading to

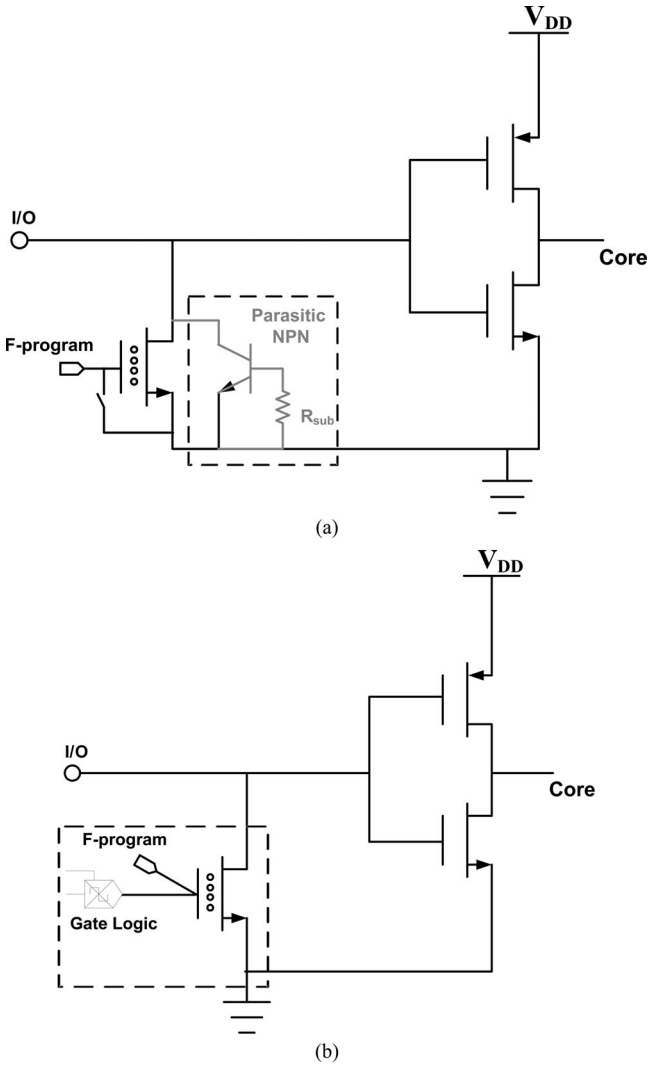

Fig. 3. Two possible ESD triggering programming and design schemes: (a) Scheme-1 depicts a typical ggNMOS NC-QD ESD protection design where an external field programming control is used to realize the ESD ΔV_{t1}. A simple antifuse may be used to separate the gate programming and the ggNMOS ESD structure. (b) Scheme-2 allows the NC-QD ESD protection in normal MOSFET conduction mode with its ESD ΔV_{t1} being enabled by both external field-programming control and embedded gate logic function.

the desired ΔV_{t1} in field designs. Several possible techniques may be used to separate the NC-QD gate programming to adjust the ESD V_{t1} and the ggNMOS ESD protection structure in field applications including a simple antifuse technique [shown in Fig. 3(a)] or a logic subcircuit unit between the gate and the source in practical IC designs, which are under investigation. In Scheme-2 as shown in Fig. 3(b), the NC-QD ESD protection structure can be connected in such a way that the NMOSFET will be turned ON into the normal MOSFET conduction mode by an ESD transient for ESD discharging operation, i.e., after the gate bias is greater than the MOSFET threshold voltage ($V_G > V_{\mathrm{th}}$), similar to a typical ESD power-clamp device in practical designs [3]. The unique feature of the new NC-QD ESD protection structure in Scheme-2 is that, by utilizing external biasing to charge/decharging the NC-QD layer, V_{th} will

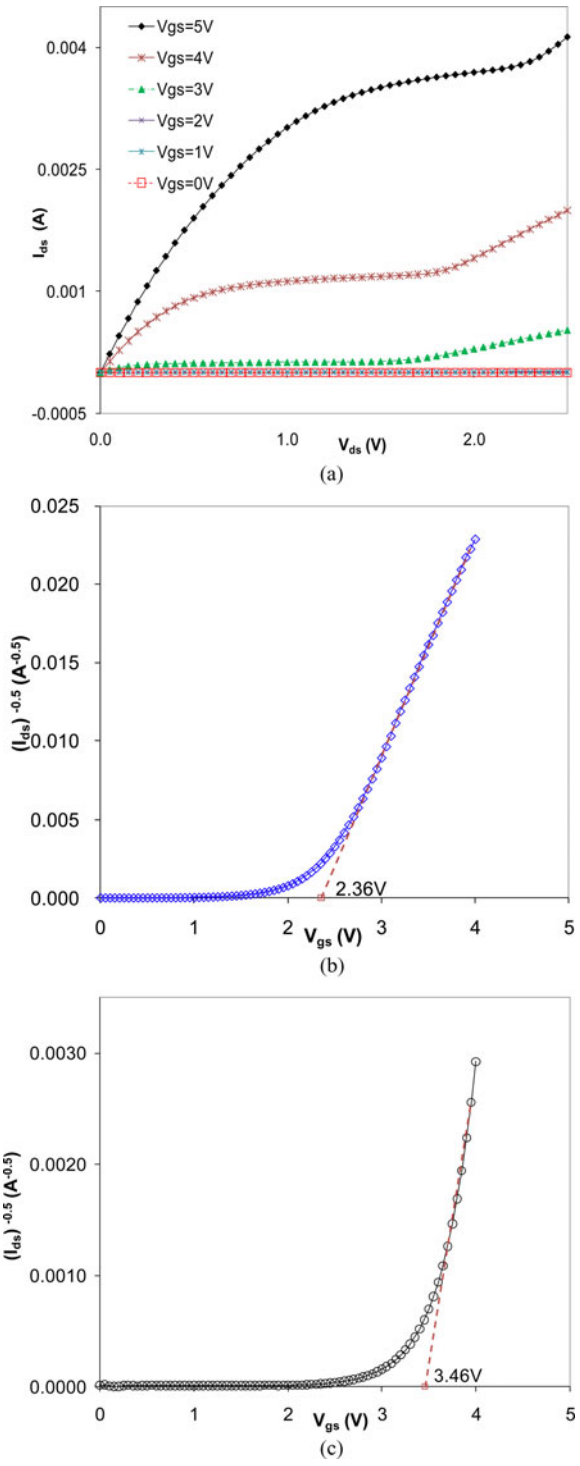

Fig. 4. Measured *I–V* characteristics for prototype NC-QD ESD protection devices show the shift of threshold voltage $\Delta V_{\rm th}$ by programming: (a) normal $I_{\rm DS}$–$V_{\rm DS}$ curve; (b) $\sqrt{I_{\rm DS}} - V_{\rm GS}$ before charging; (c) $\sqrt{I_{\rm DS}} - V_{\rm GS}$ after charging.

vary $\Delta V_{\rm th}$, which results in a tunable ESD triggering ΔV_{t1}. In addition, an embedded logic circuitry can be used to program the gate bias to the NC-QD ESD protection structure, which further controls the ESD triggering threshold of the NC-QD ESD protection structure. These two mechanisms combined together will enable a substantial ESD triggering field programmability,

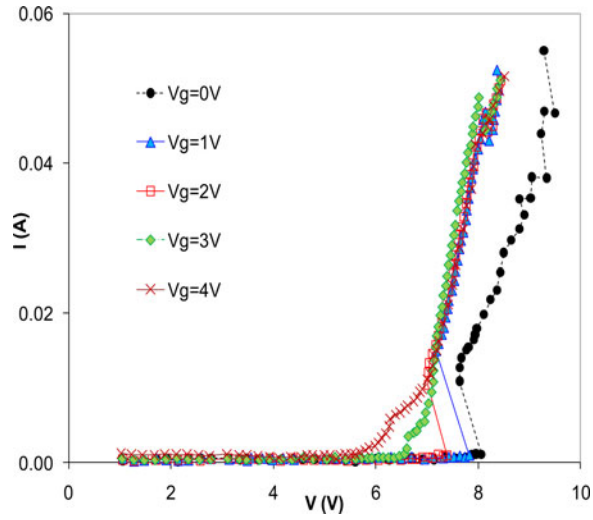

Fig. 5. Measured ESD discharging *I–V* characteristics for sample NC–QD ESD protection structures by TLP before programming show the desired ESD triggering variation, up to $\Delta V_{t1} \sim 2.46$ V, at different gate biasing V_g.

i.e., a large ΔV_{t1} for a fabricated NC-QD ESD protection structure through field programming. While this tunable-V_{t1} NC-QD ESD protection concept is experimentally verified in this study, an accurate, quantitative ΔV_G–ΔV_{t1} relationship for the new NC-QD ESD protection structures needs to be further investigated. One highly desired feature for the Scheme-2 NC-QD ESD protection is that the NC-QD ESD MOSFET will be driven into normal MOSFET conduction operation, i.e., a nonsnapback *I–V* behavior, which allows whole-chip simulation design and verification of the ESD-protected IC using SPICE simulator. Whole-chip ESD simulation using SPICE is very beneficial because lack of accurate ESD device model for snapback-based ESD protection structures has made it impossible to conduct chip scale ESD simulation using SPICE circuit level simulators and TCAD numeric simulation may be required for whole-chip ESD simulation in practical IC designs [3], [4]. In practical designs, several techniques can be used to fine-tune the ESD V_{t1}. First, the NC-QD ESD structures may be preprogrammed individually to adjust V_{t1} for different IC blocks using different $V_{\rm DD}$, which is essential to mixed-signal ICs using multiple power supplies. Second, on-chip digital programming circuitry may be used to locally program the nanocrystal dots for varying ESD V_{t1}. Third, on-chip V_G biasing can be carefully programmed for Scheme-2 NC-QD ESD structures to adjust $V_{\rm th}$, and thus control the ESD V_{t1}. Fourth, ESD V_{t1} may be adjusted by varying NC dot density for a wider V_{t1} tuning range. A new silicide-coated NC dot technique [10], [11], which enhances NC-QD charging efficiency by bandgap engineering, is used in this study for better ESD V_{t1} programming results. In future, multiple-layer NC-QD arrays may be realized to make new NC-QD ESD protection structures, which would allow even wider ΔV_{t1} for more accurate and flexible on-chip ESD protection design in field applications.

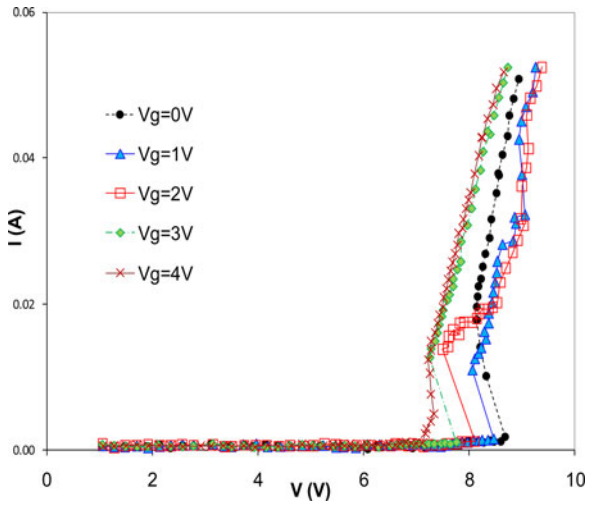

Fig. 6. Measured ESD discharging *I–V* characteristics for the sample NC-QD ESD protection structure by TLP after programming show the expected ESD triggering variation, up to $\Delta V_{t1} \sim 2.39$ V, controlled by gate biasing V_g.

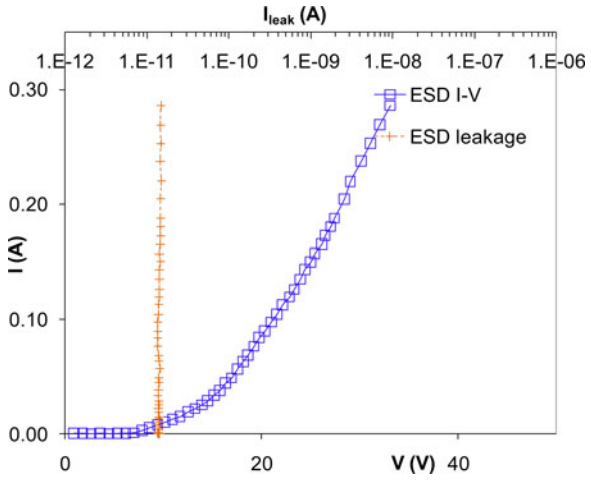

Fig. 8. Measured transient *I–V* characteristics for a sample NC-QD ESD protection structure by VF-TLP show expected ESD discharging behavior, confirming its vary fast response time to ESD pulses with an ultrashort rising time of 100 ps response, and very low leakage of ~pA level.

TABLE I
MEASURED V_{t1} AND V_h FOR SAMPLE NC-QD ESD PROTECTION STRUCTURES AT DIFFERENT GATE BIASING V_g BY TLP

	V_g (V)	0	1	2	3	4
Before Prog.	V_{t1} (V)	8.06	7.82	7.39	6.46	5.60
	V_h (V)	7.64	7.17	7.02	--	--
After Prog.	V_{t1} (V)	8.68	8.11	7.76	7.12	6.29
	V_h (V)	8.06	7.50	7.25	7.22	--

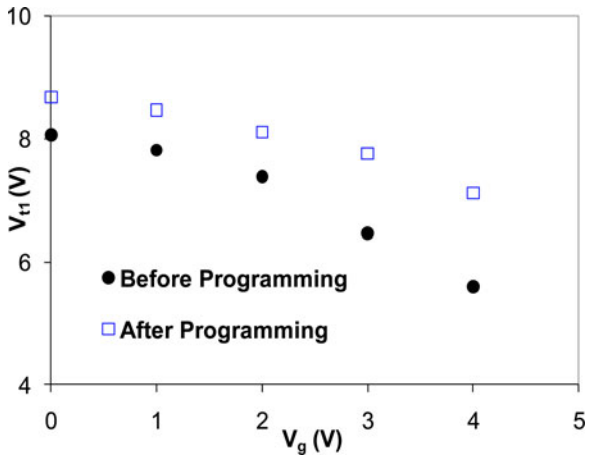

Fig. 7. Measured V_{t1}–V_G curves for sample NC-QD ESD protection devices readily show the expected ESD triggering variation behaviors, i.e., the desired ΔV_{t1}–V_G programming relationship.

III. EXPERIMENTS AND DISCUSSIONS

NC-QD ESD protection structures of varying design matrix were fabricated in a CMOS-compatible process for heterogeneous integration. A 5-nm tunneling oxide is grown on Si at 850 °C, followed by Si NC dots deposition by LPCVD at 600 °C. A 1-nm cobalt film is then deposited and annealed to form $CoSi_2$. Unreacted Co is etched off, resulting in $CoSi_2$-coated NC-QD array, covered by 20-nm control oxide. The NC dot size is 10 nm with a dot density of 4×10^{11} cm^{-2}. Both dc and transient ESD transmission line pulsing (TLP) testing were conducted. Typical NC-QD programming requires $V_G \cong 20$ V for 5 s and 50% duty cycle to charge NC-QD array. Fig. 4 gives the measured dc $I_{\rm DS}$–$V_{\rm DS}$ and $\sqrt{I_{\rm DS}} - V_{\rm GS}$ curves for sample NC-QD ESD protection devices confirming the normal MOSFET *I–V* functions. The $V_{\rm th}$ values were extracted, which clearly show the expected shift of $V_{\rm th}$, from 2.36 to 3.46 V, before and after programming. Figs. 5 and 6 show TLP testing results for HBM ESD (pulse rise time, $t_r \sim$10 ns) under varying gate biasing V_G. The extracted V_{t1} and V_h values from measurements are summarized in Table I. It readily confirms that both the ΔV_{t1}–ΔV_G programming and ΔV_{t1}–ΔV_G mechanisms, described previously, work in changing the ESD V_{t1}, which is depicted in Fig. 7. Figs. 6 and 7 readily show that, at lower V_G, the typical ESD snapback *I–V* behavior occurs due to the nanocrystal dot programming mechanism where higher V_G helps to reduce the ESD V_{t1}. However, when V_G increases to certain level, it substantially reduces V_{t1} of MOSFET, and hence results in nonsnapback MOSFET conduction (at $V_G > V_{\rm th}$) with normal *I–V* curve under ESD stressing, which is attributed to the ΔV_G–ΔV_{t1} mechanism for the Scheme-2 ESD protection. Since charging to the nanocrystal dots leads to higher $V_{\rm th}$, Figs. 5 and 6 show that the normal MOSFET conduction occurs for $V_G = 4$ V after programming compared to that occurring at $V_G = 3$ V before programming. Clearly, the bias combination of V_G, $V_{\rm th}$, and V_{t1} (i.e., ΔV_G, $\Delta V_{\rm th}$, and ΔV_{t1}) will determine the MOSFET ESD conduction mode in practical ESD protection circuit designs [12]–[15]. To examine its response to ultrafast CDM ESD surges (featuring a typical rising time of $t_r \sim 400$ ps), very fast (VF)-TLP testing (featuring a very fast rising time of $t_r \sim$ 100/200/400 ps and pulse duration $t_d \sim$ 1/2/5 ns) was conducted for the NC-QD ESD protection devices. Fig. 8 presents the measured transient

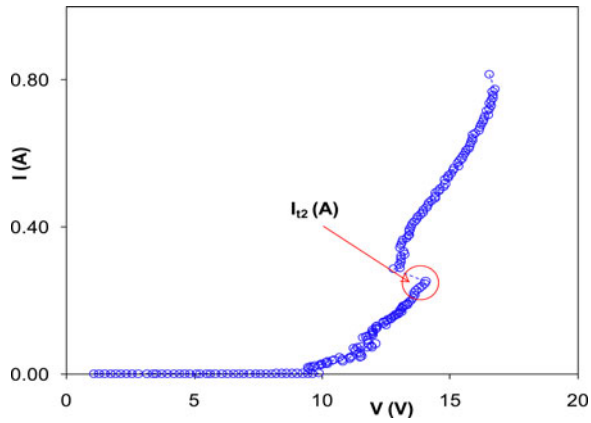

Fig. 9. Measured full transient *I–V* characteristics for a sample NC-QD ESD protection structure by TLP show its thermal breakdown threshold I_{t2}, an indicator to its ESD protection capability.

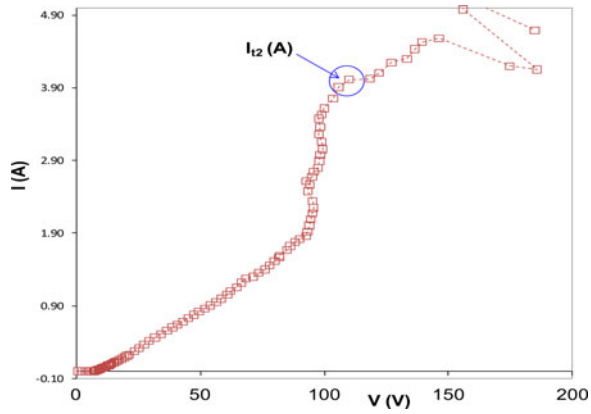

Fig. 10. Measured full transient *I–V* characteristics for a sample NC-QD ESD protection structure by VF-TLP to show its thermal breakdown threshold I_{t2}, an indicator to its ESD protection capability.

I–V and leakage for an $L = 1$ μm /W $= 1$ μm device by VF-TLP with an ultrafast ESD pulse featuring a very short rising time of $t_r = 100$ ps. It clearly shows that the new NC-QD ESD protection devices have the potential to respond to extremely fast ESD transients of as short as $t_r \sim 100$ ps and $t_d \sim 1$ ns, while achieving a very low leakage of $I_{\rm leak} \sim 14.6$ pA at a bias of 0.5 V under such ESD stressing. Figs. 9 and 10 present the full transient ESD discharging *I–V* curves for a sample $L = 1$ μm /$W = 10$ μm NC-QD ESD device by TLP and VF-TLP, respectively, which show the thermal breakdown threshold points I_{t2} for the measured new tunable ESD protection concept and mechanism. The results strongly suggest that the new NC-QD ESD protection structures have the potential to become the first field-programmable on-chip ESD protection solution to complex mixed-signal ICs down to nanonodes and shall allow fine-tune of ESD triggering in electronic systems in post-Si designs. Design optimization is on-going currently.

IV. Conclusion

A new tunneling-assist NC-QD ESD protection concept and mechanism were presented to realize field-programmable ESD triggering voltage for the first time. Prototype NC-QD ESD protection structures were designed and fabricated in a CMOS-compatible process and fully validated the tunable-V_{t1} NC-QD ESD protection concept. Experiments demonstrated fully functional NC-QD ESD protection devices achieving an adjustable ESD ΔV_{t1} of 2.5 V, very fast response to ESD pulses of $t_r \sim$ 100–400 ps and $t_d \sim$ 1–5 ns, very low leakage current of $I_{\rm leak} \sim$ 15 pA, HBM ESD protection level $I_{t2} \sim 25$ mA/μm and CDM equivalent (fast pulses of $t_r \sim$ 100 ps and $t_d \sim$ 1 ns) ESD capability of $I_{t2} \sim 400$ mA/μm for the prototype devices. Wider ESD V_{t1} range may be achieved by design optimization. The NC-QD ESD protection structures can be heterogeneously integrated into CMOS. However, more process development work is needed to optimize the add-on process module for making the NC-QD structures for CMOS integration. In addition, since the new NC-QD ESD triggering concept utilizes the electrostatic charge density inside the NC-QD layer(s) to adjust the required ΔV_{t1}; it hence allows design scalability in advanced CMOS technologies because the required ESD ΔV_{t1} may be realized by improving nanocrystal dots density through either bandgap-engineering (e.g., silicidation) or multiple NC-QD layers without changing the NC-QD ESD device sizes. Similar ESD V_{t1} programming may be expected in other ESD protection structures using various floating gate control, which is being investigated currently. It may potentially become the desired field-programmable ESD protection solution to complex mixed-signal ICs at nanonodes and shall also allow post Si ESD programmability in electronic system designs in field.

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