Nonplanar NiSi Nanocrystal Floating-Gate Memory Based on a Triangular-Shaped Si Nanowire Array for Extending Nanocrystal Memory Scaling Limit

Jingjian Ren, Bei Li, Jian-Guo Zheng, Mario Olmedo, Huimei Zhou, Yi Shi, and Jianlin Liu, *Member, IEEE*

***Abstract*—A nonplanar Flash memory architecture with ultrahigh-density ($\sim 1.5 \times 10^{12}$ cm^{-2}) NiSi nanocrystals (NCs) as the floating gate is demonstrated using a triangular-shaped Si nanowire array as the memory transistor channel. The memory device shows good programming, erasing, and retention characteristics. This result suggests that nonplanar devices can extend NC memory scaling limit.**

***Index Terms*—Anisotropic etching, Flash memory, nanocrystal (NC), nonplanar.**

I. Introduction

CONVENTIONAL Flash memory with a continuous floating gate faces increasing challenges brought by charge leakage and other scaling-related issues [1]. Si nanocrystal (NC) memory was first introduced by Tiwari *et al.* in 1995 as an alternative to continuous floating-gate memory [2] and has attracted much attention for its CMOS-compatible fabrication process and immunity to oxide defect leakage together with its promising scalability due to the discrete charge storage nodes. Tremendous efforts have been invested into NC memory research ever since, using new cell structures and new materials [3]–[8]. Nevertheless, NC density and uniformity fluctuation have arisen as a critical concern as NC memory is unexceptionally approaching its scaling limit as other counterparts do [9], [10]. NC number variation from cell to cell imposes serious constraints on overall device performance with respect to programming, erasing, memory window, and retention. Furthermore, the reducing number of NCs in ultrascaled memory cells severely limits the cell state controllability and reliability and may eventually lead to cell performance failure.

The motivation behind this letter is to explore and demonstrate a nonplanar cell structure with high-density uniform metallic silicide NC charge storage nodes in the same memory cell as a possible way to extend the scaling limit of NC memory devices without compromising the device performance. The structure of NiSi NC memory based on a triangular-shaped Si nanowire (SiNW) array is shown in Fig. 1(a). The internal structure of the gate stack on a single SiNW is shown in the magnified schematic: from bottom to top are SiNW, NC embedded between SiO_2/Al_2O_3, and Al gate finger. Fig. 1(b) shows the scanning electron microscopy (SEM) images of the as-fabricated device and the cross-sectional view of embedded triangular-shaped SiNWs. The cross section of the SiNW is a quasi-isosceles triangle with a bottom edge of 140 nm and sides of 100 nm each. The advantage exhibited by this cell structure can be understood through a comparison between the planar NC memory cell and the proposed nonplanar cell. Considering the same amount of NCs in a cell, this nonplanar cell only needs to occupy about half of the effective area of a planar device due to almost doubled surface area for NC accommodation (the angle between the planar Si (100) plane and the SiNW surface (111) is 54.7°). This will enhance the integration density of memory cells on a chip to a large extent without sacrificing the number of NCs per cell. In other words, considering the same effective cell size, the number of NCs that controls cell states is almost doubled in a nonplanar device under the same NC deposition condition. In this case, the stored charge density of the whole cell is safely maintained by more NCs, leading to less dot density variation problems, as compared with planar devices at the scaled technology node. In addition, the selection of silicide

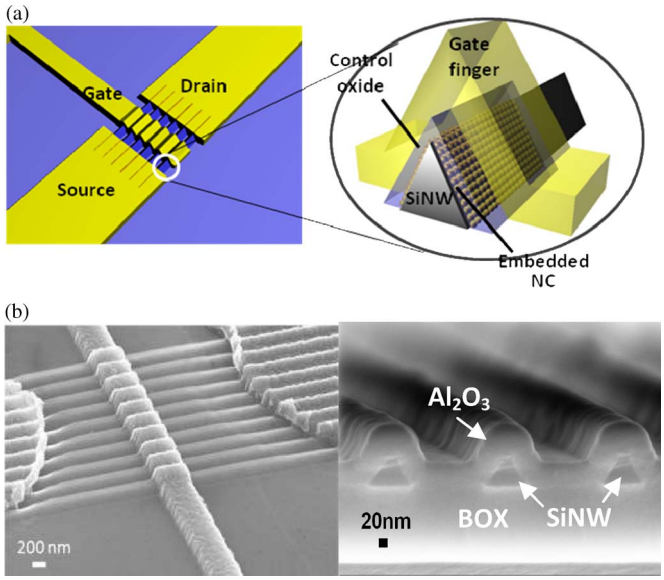

Fig. 1. (a) Schematic and (b) SEM images of triangular-shaped SiNW-array-based NiSi NC memory.

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J. Ren, B. Li, M. Olmedo, H. Zhou, and J. Liu are with the Quantum Structures Laboratory, Department of Electrical Engineering, University of California, Riverside, CA 92521 USA (e-mail: jianlin@ee.ucr.edu).

J.-G. Zheng is with the Laboratory for Electron and X-ray Instrumentation, Calit2, University of California, Irvine, CA 92697 USA.

Y. Shi is with the School of Electronic Science and Engineering, Nanjing University, Nanjing 210093, China.

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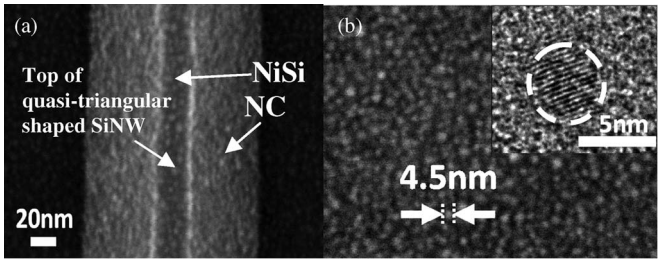

Fig. 2. (a) Top-view SEM image of NiSi NCs on a SiO_2-covered SiNW. (b) SEM image of NiSi NCs at open area. (Inset) HRTEM image of a single NC.

NCs in this letter is due to the excellent thermal stability and the large work function for long retention and enhanced device reliability [3], [6].

II. Device Fabrication

The fabrication process is described here. Starting with a commercially available silicon-on-insulator wafer (with an 88-nm p-type Si (100) active layer, Soitec, Inc.), phosphorous ion implantation was performed to dope the Si active layer for n-type NW device fabrication. The implant energy and dose were chosen to yield a uniform doping concentration of 10^{18} atoms $\cdot$ cm^{-3} to ensure a reasonable drive current and good source and drain contacts. The sample was then annealed in a nitrogen ambient at 950 °C for 60 s to activate the doping impurities. Dry thermal oxidation at 950 °C and diluted HF etching were utilized to thin down the top Si layer to around 60 nm. Line-and-space patterns along the [110] direction were created by electron-beam (e-beam) lithography, and chromium was deposited by e-beam evaporation to form a hard mask for the next etching step. A KOH solution was used to anisotropically etch the Si layer, and etching time was carefully controlled to produce a well-aligned triangular-shaped SiNW array [11]. After hard mask removal and sample cleaning, a 5-nm tunnel oxide was formed by dry oxidation of the SiNW at 850 °C and subsequent annealing at 950 °C for oxide quality enhancement. This was followed by room-temperature e-beam evaporation of a very thin layer of Ni as a catalyst for silicide NC growth. NiSi NCs were synthesized by direct vapor–solid–solid (VSS) growth at 600 °C in a low-pressure chemical vapor deposition system, using SiH_4 as the gas source [6].

The SEM image of the top view of the NC layer on a SiO_2-covered SiNW is shown in Fig. 2(a). Fig. 2(b) shows ultrahigh-density NCs at the open area of the as-grown sample. It is determined from the images that the NCs are uniformly distributed over the whole sample surface with the average size of about 4.5 nm and the density of around 1.5×10^{12} cm^{-2}. Due to the triangular shape of the NW, such high density of NCs is also ensured at the nonplanar SiNW area through the same metal catalyst deposition and VSS growth processes. The high-resolution transmission electron microscopy (HRTEM) image of a single NC in the inset shows good crystallinity of the NC. The composition of the NCs is confirmed to be NiSi by HRTEM and X-ray photoelectron spectroscopy. By employing atomic layer deposition, a 36-nm Al_2O_3 was uniformly deposited as the control oxide for the device. Then, the source and drain areas were defined by photolithography, and Ti/Au was deposited as the contacts to the highly doped SiNW array to form a junctionless transistor with no necessity of ion implantation.

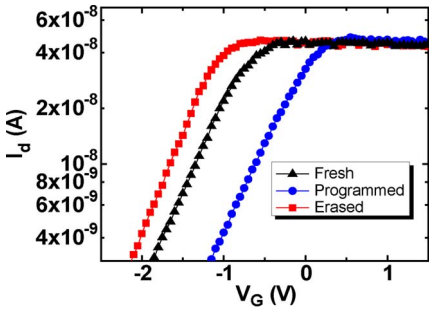

Fig. 3. Transfer characteristics of triangular-shaped SiNW-array-based NiSi NC memory at neutral, programmed, and erased states.

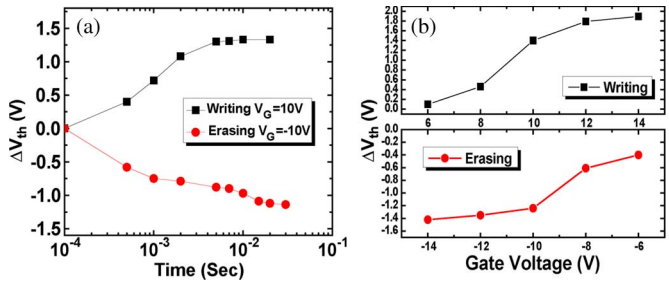

Fig. 4. (a) Time and (b) gate-bias-dependent P/E characteristics.

This type of device bypasses the challenging junction formation steps and favors ultrascaled device fabrication. A last e-beam lithography and e-beam evaporation step finalized the top-gated device fabrication by putting an Al gate finger over the multi-SiNW channel. The width of the gate finger defines the gate length on each SiNW to be 0.5 μm for each device. A control device without NCs was simultaneously fabricated for comparison.

III. Results and Discussion

An Agilent 4155C semiconductor parameter analyzer was utilized to characterize the electrical properties of the devices. Fig. 3 shows the transfer characteristics, i.e., I_d–V_g, for this memory device at neutral, programmed, and erased states. Gate biases of 7.5 and -10 V were applied for programming and erasing (P/E), respectively, both for 100 ms. The shift of the I_d–V_g curve toward the higher (lower) gate voltage side indicates the charging (discharging) of NiSi NCs with electrons. In comparison, the I_d–V_g curves of the control device shows a negligible shift under the same programming condition (not shown here), which confirms that the memory effect should be attributed to the NCs.

Fig. 4(a) and (b) show the time and gate-bias-dependent P/E characteristics of the device, respectively. As shown in Fig. 4(a), the threshold voltage shift $\Delta V_{\rm th}$ of the device increases with the P/E time under a gate bias of ± 10 V, until saturation at around 10 ms. The large window of 2.7 V indicates good P/E performance and charge storage capability. $\Delta V_{\rm th}$ as a function of the gate bias, as shown in Fig. 4(b), shows clear voltage dependence of the P/E performance under a fixed P/E time of 20 ms, which is consistent with the fact that a higher voltage promotes electron tunneling through the barrier between the floating gate (NCs) and the channel. The slightly faster speed in the programming case than in the erasing case can be ascribed to the lower tunneling barrier height that electrons see from the NW toward the NC.

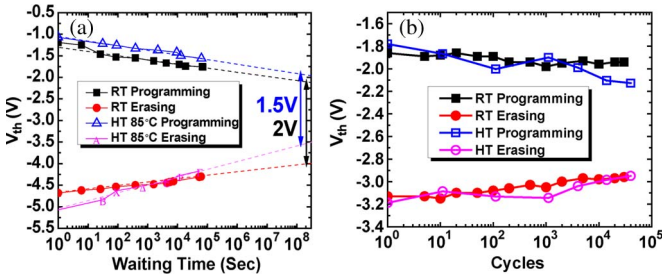

Fig. 5. (a) Retention and (b) endurance characteristics of triangular-shaped SiNW-array-based NiSi NC memory at room temperature and 85 °C.

Fig. 5(a) shows the comparison between retention characteristics at room temperature and 85 °C. Programmed and erased with ±12 V/200 ms, the device shows remained memory windows of 2 and 1.5 V for room- and high-temperature tests, respectively, when extrapolated to ten years, suggesting insignificant degradation of the retention performance in a high-temperature environment due to the robust thermal stability of metallic silicide NCs. Fig. 5(b) shows the endurance characteristics under a gate bias of ±10 V. Only very slight memory window shrinkage was observed after cycling at both room temperature and 85 °C. The similarity in endurance characteristics at room and high temperatures again indicates that no evident performance degradation of this type of device happens under a high temperature.

It should be noted that, although a strict comparison of performance among reported NC memory work is impossible due to varied device structures, NC materials/density and tunneling/control oxide materials/thicknesses, rough evaluation of the P/E efficiency and retention and endurance characteristics among different NC memory devices shows that the overall memory performance achieved with this device is very competent [4], [12]–[18]. This includes the relatively low operation voltages required in light of the large $\Delta V_{\rm th}$ exhibited, which may benefit from the particular electric field distribution due to nonplanar geometry [14], and the robustness of retention and endurance properties at both room and high temperatures, as previously described. With further process optimization, it is expected that nonplanar devices like this could achieve much more enhanced performance for future memory scaling.

IV. Conclusion

The idea of nonplanarity has been demonstrated for an NC memory cell through fabrication and characterization of a proof-of-concept device based on a triangular-shaped SiNW array. This device shows good programming, erasing, retention, and endurance performance. For scaling up cell density, follow-up work on single SiNWs with reduced sizes will be carried out to further prove that dot density variation effect is alleviated in 3-D devices and that this device architecture can be a possible way of pushing the scaling limit of NC memory devices further at the scaled memory technology nodes.

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