Temperature-dependent electron transport in highly ordered Co/Al_2O_3 core-shell nanocrystal memory synthesized with di-block co-polymers

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Di-block copolymer synthesized Co/Al_2O_3 core-shell nanocrystal (NC) capacitors were fabricated in order to study the temperature-dependent electron transport. The capacitance-voltage memory window is shown to increase proportionally with the substrate temperature, saturating at 3.5 V, at 175 °C. At elevated operating temperatures, the tunneling of electrons increases, resulting in large flatband voltage shift. Furthermore, the electron leakage of the NCs at high temperature is faster than the leakage at room temperature due to thermally assisted tunneling. The activation energy is determined by exponentially fitting the thermally dependent retention performance, which was then used to model the occupied energy levels and further elucidate the electron transport within the NC memory. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.3698322]

I. INTRODUCTION

Nonvolatile memory devices with floating-gate architectures are widely used in many of the current electronic devices, specifically flash driver, digital cameras, and memory cards.[1] Scaling limitations in conventional floating gate nonvolatile memories have led to the development of novel memory devices that allow for high density storage.[2–4] Nonvolatile memory with discrete-trap type storage nodes, particularly nanocrystal (NC) trap storage nodes, has attracted much attention as a promising candidate for future low power electronics.[5–9] New types of NC floating dots, such as double Si dots,[10] Ge nanocrystals,[11] metal[12] or metal-like[13] dots, and dielectric NCs (Al_2O_3, HfO_2, Si_4N_3, etc.),[14–16] have been proposed to achieve memory devices with long retention performance. Among these efforts, metallic NCs have some advantages over the proposed semiconductor NCs, such as higher density of states around the Fermi level with a smaller energy perturbation. Furthermore, the metallic NCs form deep quantum wells between a control oxide and a tunnel oxide due to large work functions.[17,18] Recently, several approaches to fabricate high density core-shell NC memory devices have been implemented to achieve improved performance.[19,20] Co/Al_2O_3 core-shell NC memory, using Fowler–Nordheim (FN) tunneling for program/erase (P/E) operation, has been demonstrated to achieve enhanced retention performance without sacrificing P/E speed. Uniformly distributed NCs assembled by di-block copolymer were employed in the devices, which is promising for improving device performance, scalability, and manufacturability.[20] In most nonvolatile memory works, the P/E characteristics are usually investigated at room temperature, and direct experimental observations of temperature dependent P/E characteristics are very rare.[21–24] The ambient temperature can vary significantly during operation of nonvolatile memory, therefore it is essential to investigate the temperature effect on the memory performance and to estimate the performance of a memory embedded circuit under different ambient temperatures.[25] In this paper, we report the temperature-dependent P/E and retention characteristics of di-block copolymer assembled core-shell NC nonvolatile memory.

II. EXPERIMENTS

Figure 1(a) shows the cross-section schematic of the core-shell NC metal oxide semiconductor (MOS) capacitor memory. The device consists of a 3-nm thermally grown SiO_2 layer on Si(100), a layer of Co/Al_2O_3 core-shell floating gate fabricated using a PS-B-P(4VP) di-block copolymer process of Co NCs followed by atomic layer deposition of Al_2O_3, respectively. Finally, a SiO_2 control oxide of about 15 nm was deposited using a LPCVD process and an Al metal gate contact was evaporated onto the stack. The detailed fabrication process was reported elsewhere.[20] Figures 1(b) and 1(c) show the atomic force microscope (AFM) images of the Co NCs on top of the Al_2O_3 layer with di-block copolymer and core-shell NCs, respectively. The NC arrays are well ordered with uniform size and spacing between particles, resulting in a density of $\sim 5 \times 10^{11}$ NCs/cm^2. The average diameter of the NCs is determined to be $\sim$6 nm with an average distance spacing of $\sim$14 nm.

III. RESULTS AND DISCUSSION

The MOS capacitor memories were characterized using an Agilent LCR meter at various substrate temperatures. Figure 2(a) shows typical high-frequency (1 MHz) capacitance-voltage (C-V) response using a scanning range between ± 10 V for the fabricated core-shell NC memory devices with a scan rate of 0.5 V/s. At 25 °C, the capacitor memory window of 0.8 V was achieved. As expected, increasing the temperature causes an increase of the memory

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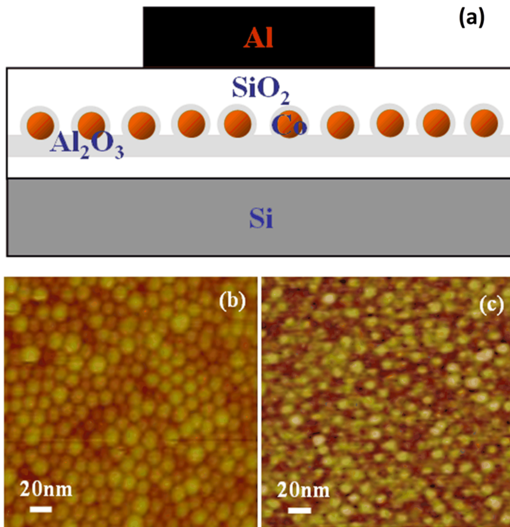

FIG. 1. (a) Schematic cross section of core-shell NC memory; (b) AFM image for Co NCs with di-block copolymer on Al_2O_3 surface; (c) AFM image for core-shell NCs.

window due to thermal energy aiding in the tunneling of electrons through the oxide layers. As the temperature increases from 100 °C to 175 °C at 25 °C intervals, a maximum memory window of 3.5 V was obtained. At 175 °C, the NC arrays become saturated and are no longer able to accept more electrons, limiting the window to 3.5 V.

Figures 3(a) and 3(b) show P/E characteristics of the core-shell NC memory measured at different P/E gate bias at 25 °C and 125 °C, respectively. As shown in Fig. 3(a), using a gate bias of 6 V, the flatband voltage shift (ΔV_{FB}) is only 0.2 V, which is believed to be caused by direct tunneling of the electrons. Increasing the gate bias to 16 V increases the ΔV_{FB} to 1.1 and 1.8 V for the two temperatures, respectively. The increase in ΔV_{FB} confirms that more electrons are activated and then injected and trapped in the NCs at higher temperatures, which are considered to be caused by thermally assisted activation. More importantly, the increase of ΔV_{FB} indicates that the programming efficiency is increased at higher temperatures. The physical process of the electron transport in the memory capacitor is illustrated in the inset of Fig. 3(a), the red color illustration shows more

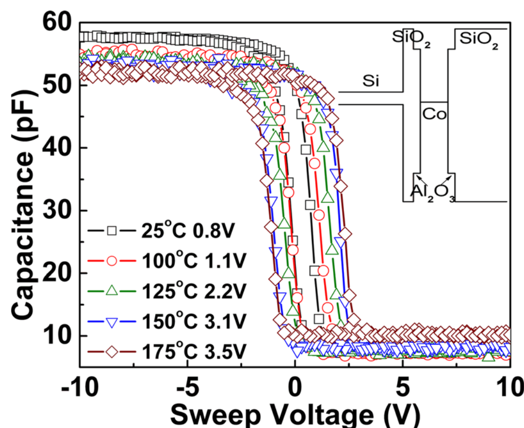

FIG. 2. C-V sweep memory window for core-shell NC memory at different temperatures. Inset is flatband diagram of the device.

electrons are activated at higher temperature. Similarly, with the application of a negative gate bias, the ΔV_{FB} increases with temperature from 1.0 to 1.3 V as shown in Fig. 3(b). Similar to the programming case, the increase of ΔV_{FB} indicates electrons are erased from the NCs at a higher rate due to the increased thermal energy of the electrons at higher temperature. The inset in Fig. 3(b) shows the band diagram depicting the erasing process, which indicates that more trapped electrons are activated and tunneling back to the substrate, leading to a large ΔV_{FB} shift. To quantitatively clarify the relation between programming/erasing speeds and temperatures, a self-consistent calculation of Schrodinger and Poisson equations was carried out to obtain the programming/erasing speeds for one electron to go through the tunneling layer at the temperature of 25 °C, 125 °C, and 175 °C and at different gate voltage, which is shown in Figs. 3(c) and 3(d), respectively. Detailed information about the self-consistent calculation can be found elsewhere.[7] The temperature is found to follow an exponential relation with programming/erasing speeds as a result of the temperature-

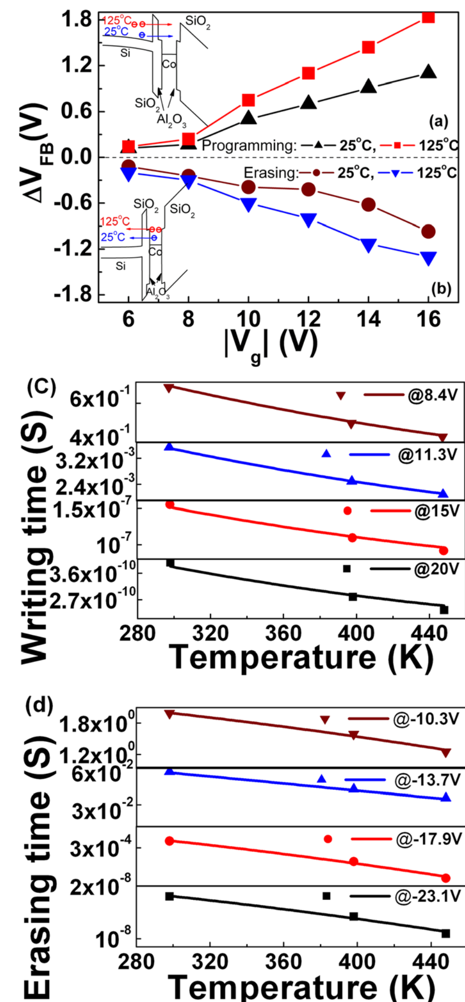

FIG. 3. (a) Programming and (b) erasing characteristics for core-shell NC memory at 25 °C and 125 °C, respectively. (c) Programming and (d) erasing speed change with temperature at different gate voltage in core-shell NC memory, respectively. In (c) and (d), symbols are simulated results, solid lines are fitting results. The fitting results show the exponential relationship between programming/erasing speed and temperature.

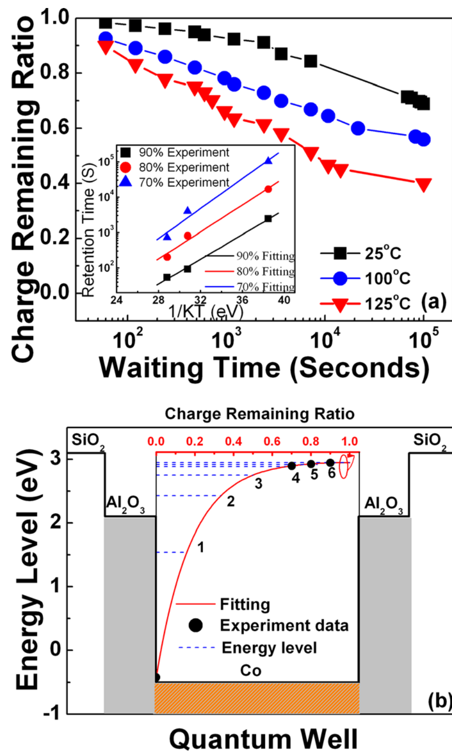

FIG. 4. (a) Retention characteristics for core-shell NC memory at different temperatures, inset image shows linear fitting of E_A. (b) Occupying energy level of stored electrons by fitting which quantitatively explains the electron transport in retention.

dependent Fermi-Dirac distribution function, which is shown as solid fitting curves. The straightforward exponential relation between temperature and programming/erasing speeds indicates the temperature assisted effect in NC nonvolatile memory device.

Figure 4(a) shows retention characteristics at 25 °C, 100 °C, and 125 °C to determine the effect of temperature on measured lifetimes. The initial flatband voltage shift for the device is 1.9 V at room temperature, 2.1 V at 100 °C, and 2.2 V at 125 °C, respectively. At room temperature, the remaining charge ratio is ~70% after 10^5 s. When the charge retention curve is extrapolated to 10 yr, the remaining charge ratio is predicted to be ~50%. Increasing the operating temperature to 125 °C, only 20% of the charge is predicted to remain in the NCs. Clearly, the retention performance degrades as temperature increases. In order to quantify this temperature dependence, the retention time τ is extracted from the charge ratio at 90%, 80%, and 70%, shown in the inset of Fig. 4(a). The inset plots τ as a function of the reciprocal of the thermal energy 1/(kT). Assuming the retention rate follows the first-order temperature dynamics, as defined by the Arrhenius equation: $\tau_r = \tau_0 e^{E_A/kT}$, it is possible to extract the activation energy, E_A, for the charge loss process from the linear fit of the exponential graph.[26] According to the fitting, the E_A was found to be 0.17, 0.19, and 0.22 eV for 90%, 80%, and 70% charge remaining ratios, respectively. According to experiment results and subsequent calculation through $\Delta V_{FB} = Q_{OX}T_{COX}/\varepsilon_{OX}$, the number of electrons stored per dot is found to be ~6. Combining the values of E_A with the quantum well depth of 3.6 eV for 0% charge remaining ratio, an exponential decay fitting is found to match the data points and the electron occupying energy levels are obtained from the fitting curve, as shown in Fig. 4(b). The high occupying energy level results in the high leakage rate after the charge was programed into the NCs. As the electron numbers decrease, the Al_2O_3 layer acts as a barrier for the electrons, preventing the leakage, yielding longer retention times and an improved performance. Nevertheless, E_A is found to follow the relation of ln(n), n is occupying electron numbers, which indicates the electron occupation in the practical device.

IV. SUMMARY

In summary, the temperature-dependent electron transport properties in an ordered Co/Al_2O_3 core-shell NC MOS memory have been studied. The memory window increases with ambient temperatures, from 0.8 to 3.5 V with the substrate temperature increased from 25 °C to 175 °C. When operated at elevated temperatures, more electrons are able to tunnel into and out of the Co NCs due to an increased thermal energy, resulting in an increase in ΔV_{FB}. Programming and erasing performance is found to follow the exponential relation with ambient temperature by self-consistent calculation and fitting. Additionally, the retention performance indicates the increased thermal energy aids the tunneling of electrons out of the NCs, decreasing the overall retention times. Considering the exponential relationship between thermal energy and the retention time, a curve was fitted based on the measured leakage ratio and E_A was extracted for the trap states. The electron occupation states, which follow the relation of ln(n) with n, the occupying electron numbers, are achieved from the temperature dependent retention result, showing clear physical mechanism of electron transport in retention.

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