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Rapid note

Realization of silicon quantum wires based on Si/SiGe/Si heterostructure

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Abstract. We report on the successful fabrication of silicon quantum wires with SiO_2 boundaries on SiGe/Si heterostructures by combining Si/SiGe/Si heteroepitaxy, selective chemical etching, and subsequent thermal oxidation. The observational result of scanning electron microscope is demonstrated. The present method provides a well-controllable way to fabricate silicon quantum wires.

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In recent years, artificially modulated silicon-based structure with reduced dimension such as silicon quantum wires (SQWRs) have attracted great interest for both potential device applications and for novel physical phenomena. Toward that goal, the first step is to establish valuable fabrication method of ultra fine SQWRs. In contrast with GaAs/AlGaAs system, however, only a few fabrication methods have been reported. Most of SQWRs were obtained using metal-oxide-semiconductor (MOS) structures where carrier confinement was achieved by electrostatic potential [1, 2]. Several authors recently reported the methods of fabricating physically confined SQWRs with SiO_2 boundaries by anisotropic chemical etching and thermal oxidation [3–5]. At the present stage, it is still requested urgently to develop advanced fabrication techniques to obtain SQWRs of high quality.

SiGe/Si heteroepitaxial film has many potential applications in silicon technology. It would be very attractive to be applied in fabricating various SQWRs and related devices due to its excellent properties such as high-quality epitaxial growth, selective etching and thermal oxidation [6, 7]. In this letter, we report on a novel method for fabricating the physically confined SQWRs based on SiGe/Si heterostructure. Here, high-quality Si/SiGe/Si heteroepitaxial film is firstly grown on silicon substrate. On the trench structures generated by lithography and reactive ion etching, the selective chemical wet etching is utilized to remove the SiGe layer and form silicon wires. Finally, thermal oxidation process is carried out to obtain expected SQWRs with SiO_2 boundaries. Thermal oxidation of silicon wires is one of the critical process in fabricating the SQWRs, which not only forms high-quality SiO_2/Si interfaces, but also smooths and reduces the lateral dimensions of the SQWRs. The observational result of scanning electron microscope (SEM) is demonstrated.

In Fig. 1, the fabrication step is illustrated. Firstly, a $Si_{0.8}Ge_{0.2}$ heteroepitaxial layer was grown on $\langle 100 \rangle$ oriented p-type 25–50 Ω cm silicon substrate by very low pressure chemical vapor deposition (VLP-CVD). The details of the growth technique have already been reported elsewhere [8]. A buffer silicon layer of 100 nm was grown between the substrate and the SiGe layer while a silicon active layer was grown on the top of the $Si_{0.8}Ge_{0.2}$ layer (Fig. 1a). Lithography technique was carried out to generate line-and-space patterns. Then, trenches were formed by using reactive ion etching (RIE) (Fig. 1b). Next, the selective chemical etchant consisting of HNO_3: CH_3COOH:HF at 25°C was used to etch the trench structures to remove $Si_{0.8}Ge_{0.2}$ layer out with the silicon wires remained (Fig. 1c). After removing the mask, the silicon wires were thermally oxidized in wet oxygen atmosphere which smooths the surface of the silicon wires and reduces the lateral dimensions to form expected SQWRs. Finally, the thermal oxidation in dry oxygen was carried out to obtain high-quality SiO_2/Si interfaces (Fig. 1d).

Figure 2 shows cross section SEM image of silicon nanostructures fabricated in this work. As seen from Fig. 2a, silicon wires with lateral dimensions of about 240 nm are prepared by the selective chemical wet etching. The top layer above the silicon wire is the mask. In the last several years, the selective chemical etching techniques for SiGe/Si heteroepitaxial films have been developed quickly. Among many selective chemical etchants, it has been demonstrated that the solution of HNO_3:CH_3COOH:HF was a very good etchant in thinning SiGe nanostructures [9]. Through the selective chemical etching, the $Si_{0.8}Ge_{0.2}$ layer round the trench is removed out and

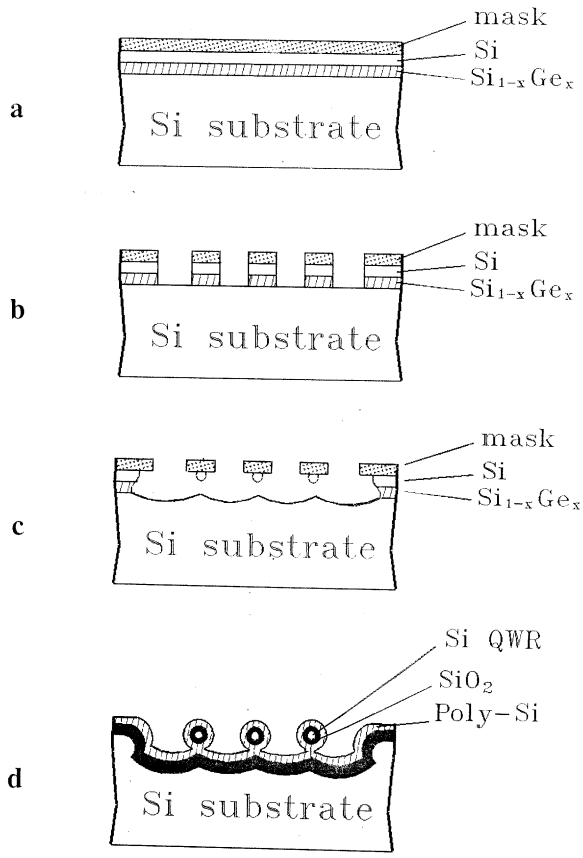

Fig. 1. Fabrication step of SQWRs. **a** Si/SiGe/Si heteroepitaxy by VLP/CVD **b** Mask pattern and shallow trench formation **c** Selective chemical etching **d** Thermal oxidation

silicon active layer is narrowed to form silicon wire. Subsequently, two steps of wet and then dry oxidation are carried out to generate ultra fine SQWRs. Here, the wet oxidation at low temperatures offers an important opportunity for realizing ultra fine SQWRs based on the present SiGe/Si nanostructure. Though the SiGe layer below the silicon wires is completely etched away after selective chemical etching, it still remains at another part of the sample. Hence, the oxidation at high temperatures above 850°C is forbidden because of the thermal stability of SiGe alloy. In addition, the dry oxidation at low temperatures is not practical because of the length of time it takes to narrow silicon wires to expected lateral dimensions. Subsequent dry oxidation after wet oxidation in this experiment is used to obtained high-quality Si/SiO_2 interface. Figure 2b shows the cross sectional SEM image of a SQWR with circular cross section embedded in the SiO_2 after the thermal oxidation. In order to clearly distinguish the SQWRs from circumstances, the sample was deposited a polysilicon film on SQWRs by the VLP-CVD reactor, and then was back-side polished and cleaved. The cleaved faces were delineative etched with a diluted HF for several minutes. This facilitated differentiation of the SQWR and oxide. The space vacated by the oxide now appeared as a dark strip sandwiches between two bright areas of silicon and polysilicon. As shown in Fig. 2b, the lateral line width of the SQWR is about 40 nm here.

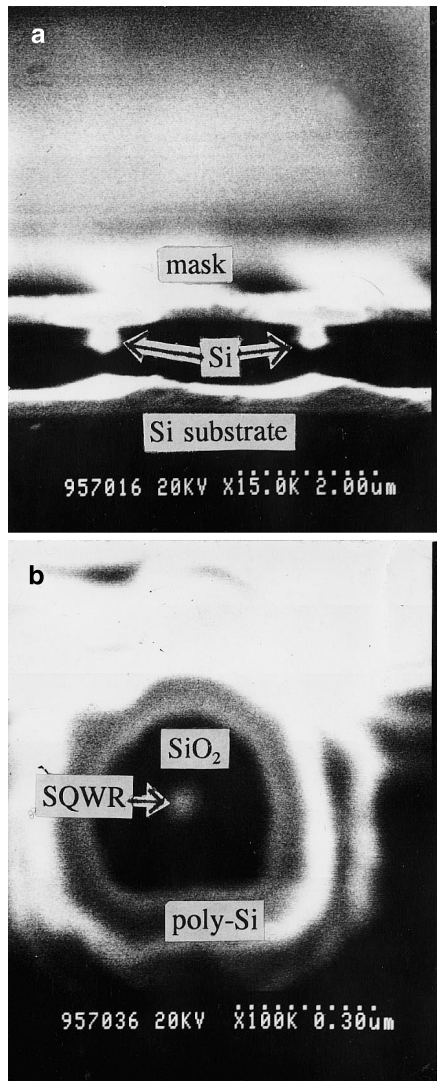

Fig. 2. Cross-sectional SEM image of **a** As-etched silicon wires **b** Thinned SQWR

In summary, we have successfully fabricated arrays of SQWRs with SiO_2 boundaries using the selective chemical etching of SiGe over Si and subsequent thermal oxidation technique based on Si/SiGe/Si heterostructure. Excellent results are evidenced by SEM. It is found that the lateral dimensions of SQWRs can be well controlled by the selective chemical etching and thermal oxidation process. This research clearly show the success of SiGe/Si heteroepitaxy, selective chemical wet etching and thermal oxidation as a very valuable method for fabricating SQWRs.

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