Solid-State Electronics 67 (2012) 23–26

Contents lists available at SciVerse ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

High-density NiSi nanocrystals embedded in Al_2O_3/SiO_2 double-barrier for robust retention of nonvolatile memory

Jingjian Ren [a], Bei Li [a], Jian-Guo Zheng [b], Jianlin Liu [a,*]

[a] Quantum Structures Laboratory, Department of Electrical Engineering, University of California, Riverside, CA 92521, USA
[b] Calit2 Microscopy Center and Materials Characterization Center, The California Institute for Telecommunications and Information Technology, University of California, Irvine, CA 92697-2800, USA

ARTICLE INFO

Article history:
Received 22 April 2011
Received in revised form 28 June 2011
Accepted 27 July 2011
Available online 27 August 2011

The review of this paper was arranged by A. Zaslavsky

Keywords:
Nanocrystal memory
NiSi
Al_2O_3/SiO_2 double-barrier
Vapor–solid–solid growth

ABSTRACT

NiSi nanocrystals of high density and good uniformity were synthesized by vapor–solid–solid growth in a gas source molecular beam epitaxy system using Si_2H_6 as Si precursor and Ni as catalyst. A metal–oxide–semiconductor memory device with NiSi nanocrystal–Al_2O_3/SiO_2 double-barrier structure was fabricated. Large memory window and excellent retention at both room temperature and high temperature of 85 °C were demonstrated.

1. Introduction

Nonvolatile memories with discrete charge storage nodes have been investigated extensively during the past decade. Since it was pioneered by Tiwari in 1995 [1], Si nanocrystal (NC) floating gate memory has been nominated as a promising replacement of conventional flash memory thanks to its immunity to defect-related charge leakage and potential to exceed flash scaling limit. Both academia and industry have also invested tremendous efforts into research of other NC memories, exploring new materials and novel gate structures for future flash memory [2–9]. Metal silicide NCs, with high density of states and robust thermal stability, have attracted much attention since they were proposed as good candidates to improve NC memory performance [10] and much work has been done to explore this material for nonvolatile memory application [11–18]. As an alternative way of improving memory performance, NC core–shell structure with additional barrier layer as floating gate has been developed and adopted by researchers. For example, metal and semiconductor NC core with oxide shell synthesized by various methods such as laser irradiation induced native oxidation [19], micelle dipping [20], chemical vapor deposition and annealing [21] and pulsed laser deposition [22] were reported.

In this paper, we report a metal–oxide–semiconductor capacitor memory device with an engineered floating gate similar to core–shell structures. The floating-gate structure consists of a layer of high-density vapor–solid–solid (VSS) induced NiSi NCs by gas source molecular beam epitaxy (GSMBE) embedded in-between two Al_2O_3 thin barriers deposited by atomic layer deposition (ALD). Fig. 1a shows a schematic diagram of the device structure. The Al_2O_3/NiSi NC/Al_2O_3 floating gate is sandwiched by a control oxide layer and a tunnel oxide layer. Fig. 1b shows the flat energy band diagram of the memory device. The Fermi-level of NiSi NC with a work function of 4.7 eV [23] is aligned within the mid-gap of bulk Si. The conduction band offset between NiSi and Al_2O_3 (electron affinity 1.35 eV, Ref. [24]) is as high as 3.35 eV. The benefit of using additional Al_2O_3 barrier layers is two folds. First, it is to minimize diffusion of Ni metal atoms into SiO_2 tunneling layer during high temperature process to reduce the charge leakage paths for prolonged retention. Second, it is to maintain programming efficiency and improve retention performance. Energy band diagrams of programming and retention states are illustrated in Fig. 1c. During programming, gate bias is applied so that electrons can be pulled into NCs by Fowler–Nordheim tunneling. Because of the high-K property of Al_2O_3, electric field concentration effect [25] makes most of the voltage drop on SiO_2 layer. In addition, since the barrier height of Al_2O_3 layer is lower than that of SiO_2, electrons do not actually have to go through the barrier of Al_2O_3 but only the thin SiO_2 tunnel barrier to reach the NC. Hence, it is believed that this structure has

* Corresponding author. Tel.: +1 951 827 7131; fax: +1 951 827 2425.
E-mail address: jianlin@ee.ucr.edu (J. Liu).

0038-1101/$ - see front matter © 2011 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2011.07.016

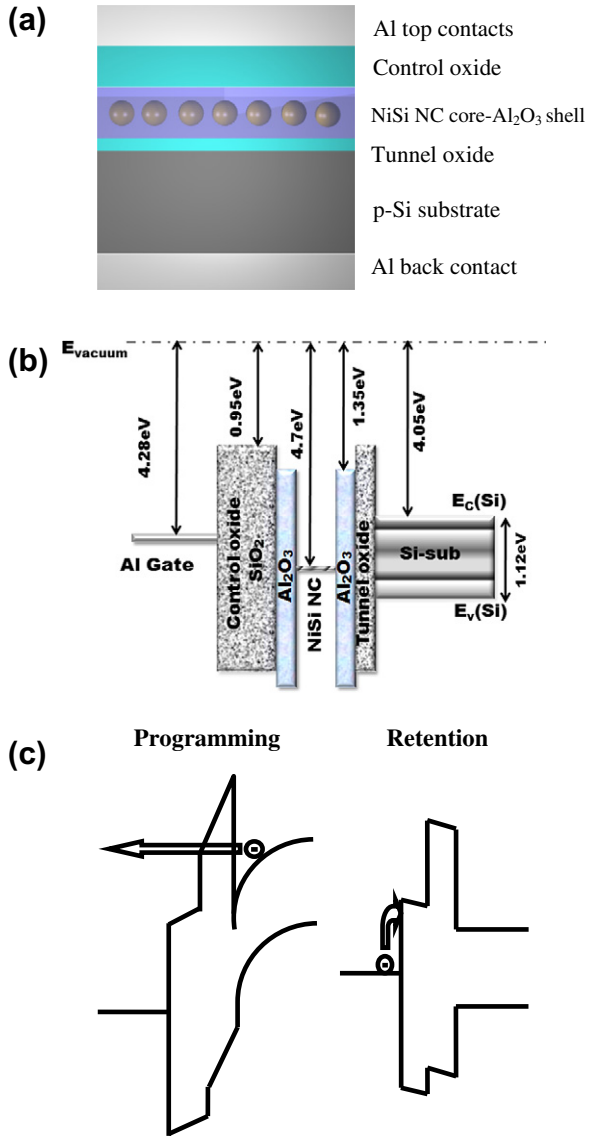

Fig. 1. (a) Schematic of device structure; (b) flat energy band diagram of NiSi NC–Al_2O_3 floating-gate memory; and (c) energy band diagram at programming and retention states.

the ability to maintain the efficiency of programming operation compared to the structure without Al_2O_3. On the other hand, in retention state, electrons are kept in the deep quantum well formed by Al_2O_3/NiSi NC/Al_2O_3 structure. In this case, electrons see a barrier of both Al_2O_3 and SiO_2 and the total barrier thickness is increased. Therefore, robust retention characteristics are expected for this Al_2O_3/NiSi NCs/Al_2O_3 floating-gate memory device combining metallic silicide NCs with double-barrier structure.

2. Device fabrication

Device fabrication starts with a pre-cleaned p-type Si (1 0 0) substrate. A thin thermal oxide of 3 nm was grown on the substrate at 850 °C. This was followed by 2.5 nm Al_2O_3 deposition using ALD. A very thin layer of Ni was coated on the sample by room temperature electron-beam evaporation as catalyst and the sample was immediately transferred into a custom-built GSMBE system for subsequent silicide NC synthesis. Disilane (Si_2H_6) was used as the Si precursor to perform VSS growth at 600 °C, which

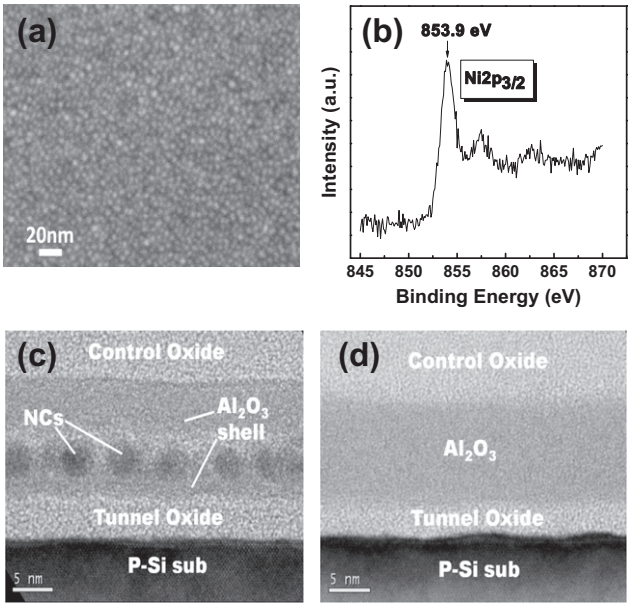

Fig. 2. (a) SEM image of high-density NiSi NCs; (b) XPS spectrum of NiSi NCs on Al_2O_3/SiO_2/Si substrate; (c) cross-sectional TEM image of NiSi NC–Al_2O_3 floating-gate memory device; and (d) cross-sectional TEM image of the control sample.

is a temperature much lower than the eutectic temperature between Ni and Si of 964 °C [26]. Growth conditions (i.e. growth time, gas source flux) were calibrated to achieve reliable high-density ultra-uniform NCs growth over the whole sample surface. After NiSi NCs formation, another thin Al_2O_3 layer of 4.5 nm was deposited

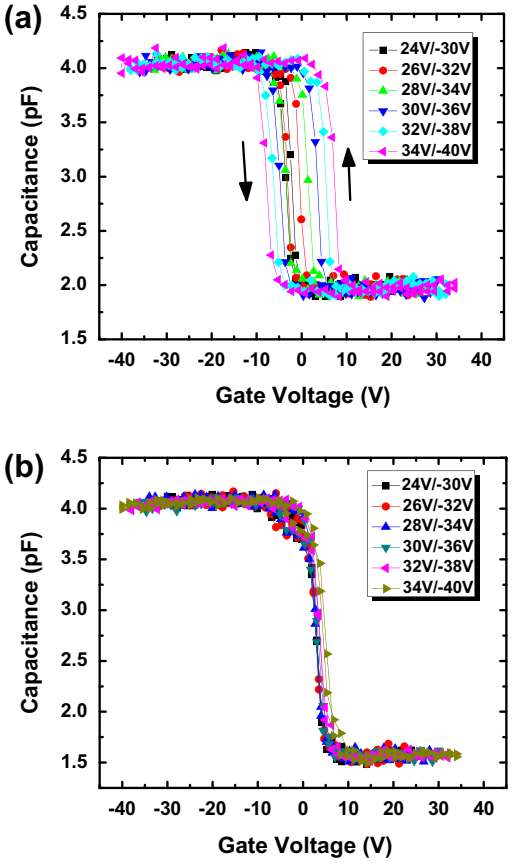

Fig. 3. C–V sweep of (a) NiSi NC–Al_2O_3 floating-gate memory device and (b) control device under different scanning gate voltages.

on top by ALD to form the Al_2O_3/NiSi NC/Al_2O_3 structure. Finally, 25 nm SiO_2 was deposited as control oxide in a low pressure chemical vapor deposition (LPCVD) system and Al was evaporated onto the front and back side of the sample as contacts for the memory capacitors. Control device without NC embedded in Al_2O_3 and NC device without Al_2O_3 were fabricated simultaneously for comparison.

3. Results and discussion

Fig. 2a shows a scanning electron microscopy (SEM) image of the as-grown NCs on Al_2O_3 surface. The average size of uniformly distributed NCs over the whole sample surface is about 4.5 nm and the density is around 1.5×10^{12} cm^{-2}. X-ray photoelectron spectroscopy (XPS) was utilized to determine the chemical nature of the NCs. Fig. 2b shows the XPS result of Ni $2p_{3/2}$ for the sample before top Al_2O_3 coverage. The binding energy peak found at 853.9 eV indicates that the nature of NC is NiSi [27]. Fig. 2c and d shows the cross-sectional transmission electron microscopy (TEM) images of the NC core–shell memory device and the control device without NC, respectively, where the interfaces are edge-on and the thickness of each layer in the devices could be measured directly from the images. The TEM images indicate that the interfaces are flat, and layer thicknesses are consistent with the designed ones, as mentioned above.

Fig. 3a and b shows high-frequency (1 MHz) capacitance–voltage (C–V) sweep characteristics of NiSi NC–Al_2O_3 floating-gate memory and its non-NC control device, respectively. With gate voltage increasing from 24 V/-30 V to 34 V/-40 V, the memory window increases from 1.4 V to 15 V, suggesting that the memory effect is due to the NC storage rather than defect/interface state charging. The large memory window also suggests high charge storage capability of the NiSi NCs. In comparison, with the same gate voltage sweeping range, almost no memory window was observed in the control device without NCs, which confirms that memory window shown by the core–shell memory device is attributed to charge storage in the NCs. The high voltage required for C–V sweeping here is due to the thick control oxide layer deposited by LPCVD. With optimized device geometry, it is expected that lower gate voltage operation and shorter programming/erasing time can be achieved.

Fig. 4a shows flat-band voltage shift (ΔV_{FB}) as a function of programming/erasing time under different gate voltages. Programming was conducted by biasing the gate with a positive voltage while a negative voltage was applied for erasing. Clear time dependence of ΔV_{FB} was observed in both programming and erasing case for gate voltage ±21 V to ±24 V. The lower speed of erasing than that of programming is due to the deep quantum well formed in the Al_2O_3/NiSi NC/Al_2O_3 structure, which makes electron see higher and thicker barrier in erasing. It should also be noticed from the curves that higher voltage results in larger ΔV_{FB}, suggesting a voltage-dependent programming/erasing behavior of the memory device. Fig. 4b shows the ΔV_{FB} and number of electrons per NC as a function of writing voltage. The charge stored per unit area in a device is calculated from: $Q = (\varepsilon_{SiO_2}/d_{SiO_2})\Delta V_{FB}$, where ε_{SiO_2} is the dielectric constant of SiO_2, d_{SiO_2} is the equivalent control oxide thickness of the MOS device, which is 27 nm in this work, and ΔV_{FB} is the V_{FB} shift between fresh state and programmed state. The charge number per NC is calculated from: # of electrons/dot = Q/Dq, where D is the NC density, which is 1.5×10^{12} cm^{-2} here and

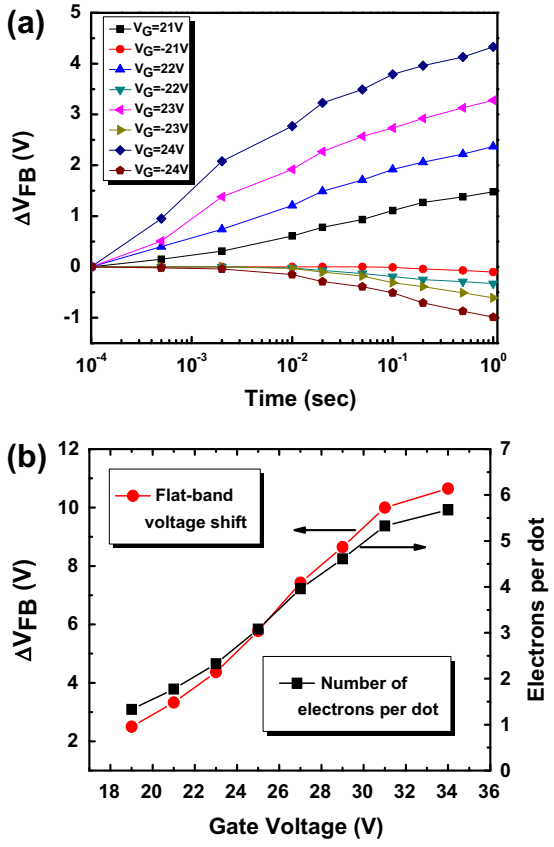

Fig. 4. (a) Transient characteristics of NiSi NC–Al_2O_3 floating-gate memory under different gate programming /erasing voltages and (b) flat-band voltage shift and number of electrons per dot as a function of gate bias.

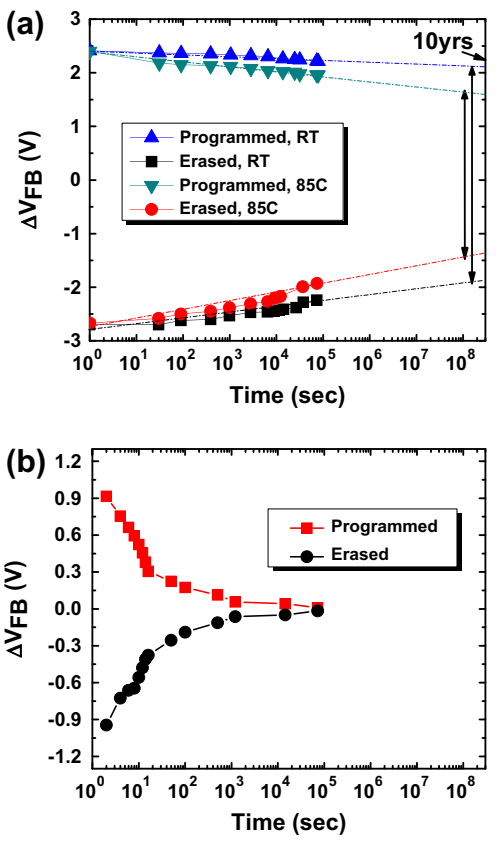

Fig. 5. (a) Retention characteristics of NiSi NC–Al_2O_3 floating-gate memory at room temperature and 85 °C and (b) retention characteristics of NiSi NC memory without Al_2O_3 barrier layer.

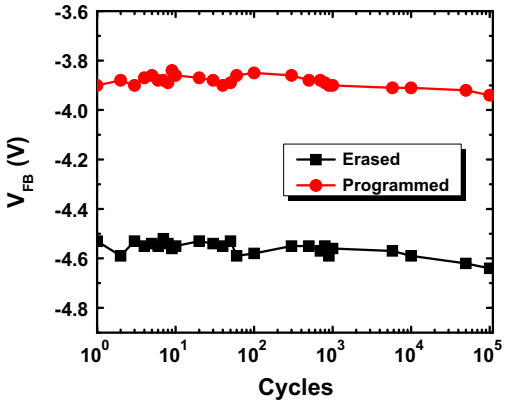

Fig. 6. Endurance characteristics of NiSi NC–Al_2O_3 floating-gate memory up to 10^5 cycles.

q is the electron charge. More than 5 electrons can be injected into each NC on average before saturation, indicating good charge holding capability of NiSi NCs similar to other metallic silicide NCs [16].

Fig. 5a shows retention characteristics of NiSi NC–Al_2O_3 floating-gate memory at room temperature and 85 °C, respectively. The device was programmed at 19 V/3 s and erased at −22 V/3 s and ΔV_{FB} as a function of waiting time is plotted. Up to 10^5 s, the charge loss ratio is only 10% for room temperature testing and 24% for high temperature testing. When extrapolated to 10 years, the curves show that there is still 80% and 60% charge maintained in the device, respectively. In contrast, 10-year charge remaining ratios between 60% and 80% were observed at room temperature only in other core–shell or NC-only device structures [17–20], suggesting that this NiSi NC/Al_2O_3/SiO_2 double-barrier floating-gate memory has the capability to achieve robust retention. Fig. 5b shows room-temperature retention characteristics of control NiSi NC memory without Al_2O_3 barriers. The memory window was almost closed completely after 10^5 s, indicating that the charge stored in NCs was lost at a very fast rate. As mentioned before, the diffusion and segregation of Ni metal atoms into SiO_2 tunneling layer during high-temperature NiSi synthesis process accounts for the fast leakage of charges and much worse retention properties. With an additional Al_2O_3 barrier, this problem has been effectively solved.

Fig. 6 shows endurance characteristics of the device. Programming/Erasing voltage of ±20 V was used to test the cycling performance. The small memory window opened is due to short pulses used in contrast to the long writing/erasing time and high voltage required by this device. It is evident that up to 10^5 cycles, the device stressed by such high gate bias keeps the window with almost no degradation, suggesting good endurance properties.

4. Conclusions

NiSi NCs of high density and good uniformity were synthesized by VSS growth in a GSMBE system using Si_2H_6 as Si precursor, based on which a nonvolatile memory with Al_2O_3/NiSi NC/Al_2O_3structure as floating gate was fabricated and characterized. The memory device exhibits large memory window, robust retention at both room temperature and high temperature of 85 °C, and good endurance. Further device geometry optimization of using thinner control oxide and varied Al_2O_3 thickness may be carried out to achieve low voltage operation as well as good transient performance. Memories with this structure can be a promising candidate for future flash memory application.

Acknowledgements

This material is based on research sponsored by DARPA/Defense Microelectronics Activity (DMEA) under agreement number H94003-10-2-1003 and the National Science Foundation (NSF) DMR-0807232. Authors acknowledge the use of FEI quanta 3D FEG dual-beam instrument and CM-20 TEM in Calit2 microscopy Center and Materials Characterization Center at UC Irvine for cross-sectional TEM sample preparation and diffraction contrast imaging.

References

[1] Tiwari S, Rana F, Chan K, Shi L, Hanafi H. Appl Phys Lett 1996;69:1232.
[2] Liu Z, Lee C, Narayanan V, Pei G, Kan EC. IEEE Trans Electron Dev 2002;49:1606.
[3] She M, King TJ. IEEE Trans Electron Dev 2003;50:1934.
[4] Chen Jing Hao, Wang Ying Qian, Yoo Won Jong, Yeo Yee-Chia, Samudra G, Chan DS, et al. IEEE Trans Electron Dev 2004;51:1840.
[5] Lee Jong Jin, Kwong Dim-Lee. IEEE Trans Electron Dev 2005;52:507.
[6] Lee Jong Jin, Harada Yoshinao, Pyun Jung Woo, Kwong Dim-Lee. Appl Phys Lett 2005;86:103505.
[7] Li Bei, Liu Jianlin, Liu GF, Yormoff JA. Appl Phys Lett 2007;91:132107.
[8] Lo YS, Liu KC, Wu JY, Hou CH, Wu TB. Appl Phys Lett 2008;93:132907.
[9] Jang J, Choi C, Lee JS, Min KS, Lee J, Kim DM, et al. Semicond Sci Technol 2009;24:115009.
[10] Zhu Yan, Zhao Dengtao, Li Ruigang, Liu Jianlin. Appl Phys Lett 2006;88:103507.
[11] Kim JH, Yang JY, Lee JS, Hong JP. Appl Phys Lett 2008;92:013512.
[12] Jang YS, Yoon JH, Elliman RG. Appl Phys Lett 2008;92:253108.
[13] Chen WR, Chang TC, Yeh JL, Sze SM, Chang CY. Appl Phys Lett 2008;92:152114.
[14] Hu CW, Chang TC, Liu PT, Tu CH, Lee SK, Sze SM, et al. Appl Phys Lett 2008;92:152115.
[15] Kim Joo Hyung, Yang Jung Yup, Lee Jun Seok, Hong Jin Pyo. Appl Phys Lett 2008;92:013512.
[16] Li Bei, Ren Jingjian, Liu Jianlin. Appl Phys Lett 2010;96:172104.
[17] Jang Yoo-Sung, Yoon Jong-Hwan. IEEE Trans Electron Dev 2009;56:12.
[18] Chen Wei-Ren, Chang Ting-Chang, Yeh Jui-Lung, Sze SM, Chang Chun-Yen. Appl Phys Lett 2008;92:152114.
[19] Lee Jun Seok, Yang Jung Yup, Hong Jin Pyo. Appl Phys Lett 2009;95:052109.
[20] Kim Chung-Jin, Choi Sung-Jin, Ryu Seong-Wan, Kim Sungho, Chang Jae-Joon, Bae SuHak, et al. Nanotechnology 2010;21:125202.
[21] Liu Hai, Winkenwerder Wyatt, Liu Yueran, Ferrer Domingo, Shahrjerdi Davood, Stanley Scott K, et al. IEEE Trans Electron Dev 2008;55:3610.
[22] Yuan CL, Lee PS. Nanotechnology 2008;19:355206.
[23] Bucher E, Schulz S, Lux-Steiner MCh, Munz P. Appl Phys A 1986;40:71.
[24] Ding Shi-Jin, Zhang Min, Chen Wei, Zhang David Wei, Wang Li-Kang. J Electron Mater 2007;36:253.
[25] Lee Chang-Hyun, Hur Sung-Hoi, Shin You-Cheol, Choi Jeong-Hyuk, Park Dong-Gun, Kim Kinam. Appl Phys Lett 2005;86:152908.
[26] Kang Kibum, Kim Cheol-Joo, Jo Moon-Ho. J Appl Phys 2009;105:122407.
[27] Cao Yu, Nyborg Lars, Jelvestam Urban. Surf Interface Anal 2009;41:471.