Vapor–Solid–Solid Growth of $NiSi_2$ Nanocrystals for Memory Application

Bei Li, Jianlin Liu, *Member, IEEE*, Reuben D. Gann, Jory A. Yarmoff, and Yu Zhu

***Abstract*—$NiSi_2$ nanocrystals were synthesized by vapor–solid–solid process, introducing SiH_4 onto Ni catalyst dots on a SiO_2 substrate, for nonvolatile memory applications. Electron microscopy was used to characterize the morphology and X-ray photoelectron spectroscopy characterization confirmed the nature of these $NiSi_2$ nanocrystals. MOSFET memory with $NiSi_2$ nanocrystal as floating gate was fabricated and fast programming/erasing speed, long retention, and 10^5 times of operation endurance performances were demonstrated.**

***Index Terms*—$NiSi_2$ nanocrystals, nonvolatile memory, vapor–solid–solid.**

I. Introduction

In recent years, the growth and device applications of nanowires (NWs) by a vapor–liquid–solid (VLS) method [1]–[5] and a vapor–solid–solid (VSS) method [6]–[8] attracted extensive attention. Both methods begin with metal catalyst dots on a substrate in the liquid, and solid form, respectively. The introduction of vapor phase precursors changes the nature of these dots from metal to silicide alloy, which acts as an effective catalyst. Further introduction of gas molecules results in the growth of NWs under these catalyst dots. In comparison with these studies on NWs, little research has been focused on their original stages, i.e., the nucleation catalyst seeds and their potential applications. In this paper, we report VSS growth of $NiSi_2$ nanocrystals (NCs) and demonstration of their nonvolatile memories.

The cross section of the device structure is schematically shown in Fig. 1(a), where $NiSi_2$ NCs are embedded between control and tunnel oxides. The device operates by sensing the threshold voltage shift under programmed and erased states.

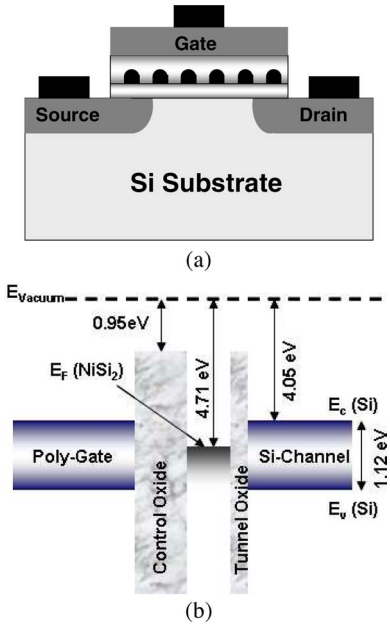

Fig. 1. (a) Device schematic cross section of $NiSi_2$ NC memory and (b) flat band diagram of $NiSi_2$ NC memory.

Two operation schemes were carried out on the devices here. The first one is Fowler–Nordheim (FN) charging mechanism, in which programming and erasing are realized by biasing the gate with a positive and negative pulse, respectively. Under programming, electrons in the inversion region of the substrate tunnel through the tunnel oxide and store in the $NiSi_2$ NCs, leading to the increase of threshold voltage compared to fresh state. Erasing process is opposite. Under a negative bias on gate, electrons in the NCs tunnel back to the channel so that the threshold voltage shifts back. The second programming scheme, hot carrier injection (HCI), was also utilized to transfer electrons from the channel to floating gate near the drain side only. Generally, silicide NCs are better than both Si NCs and metal NCs for memory applications. One of the reasons that $NiSi_2$ NCs is better than Si NCs arises from the fact that $NiSi_2$ is a metallic material with good thermal stability. As can be seen from Fig. 1(b), the Fermi level of $NiSi_2$ locates $\sim$0.66 eV below the conduction band of Si, which means a higher confinement barrier for electrons in comparison with those Si NCs [9]. This is translated into a much longer retention time in the $NiSi_2$ NC memory. Furthermore, due to metallic nature of $NiSi_2$ NCs, electrical coupling between floating gate and channel is stronger, leading to higher programming/erasing speed. Compared with pure metal NCs for memory applications [10]–[13], silicide NCs are more thermally stable. $TiSi_2$ [14], $CoSi_2$ [15], [16], and NiSi [17] NCs

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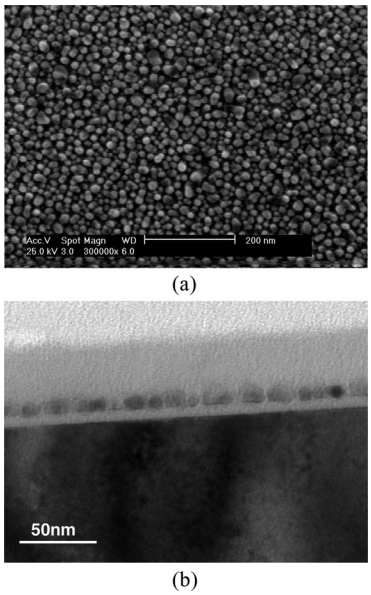

Fig. 2. (a) SEM image of $NiSi_2$ NCs on a SiO_2/Si substrate, with dot density of about 3×10^{11} cm^{-2} and (b) TEM image of $NiSi_2$ NCs embedded in a SiO_2 matrix. The size of the nanocrystals is about 7–10 nm.

have been synthesized by other methods, which have a common process, i.e., high-temperature annealing. Here, $NiSi_2$ NCs are synthesized by VSS at relatively low temperature of around 600 °C for nonvolatile memory applications. Plenty of metals can be used for VSS process to synthesize silicide NCs; therefore, work function engineering is possible to optimize memory device performance. The selection of Ni catalyst in this paper is also considered for its full compatibility with Si complementary metal–oxide–semiconductor technology.

II. Device Fabrication and Characterization

The $NiSi_2$ NCs growth and MOSFET memory device fabrication start with a p-Si (1 0 0) substrate. Local oxidation of silicon process was used to electrically isolate devices. Field oxide and nitride were grown sequentially followed by photolithography and reactive ion etching to define and expose the active region. A thin oxide of ∼5 nm was thermally grown at 850 °C for 5 min, followed by a brief N_2 *in situ* annealing at the same temperature to solidify the tunnel oxide. Temescal BJD 1800 e-beam evaporator was used to deposit 1-nm nickel (Ni) film as the catalysts for the formation of silicide dots. After metal deposition, the wafer was immediately transferred to a low-pressure chemical vapor deposition (LPCVD) system. The metal film converted to nanoparticles as the furnace was heated to the growth temperature of 600 °C, and then, SiH_4 gas of 100 sccm was introduced and diffused into the nanoparticles, leading to the formation of silicide NCs. The growth temperature is below $NiSi_2$ eutectic temperature [18]; therefore, the growth mechanism is VSS rather than VLS. The growth time is set to be 15 s to avoid NW growth. Control oxide of 20 nm and polysilicon of 300 nm were deposited sequentially followed by source/drain/gate patterning. Phosphorus ion implantation was performed on the polygate along with the source/drain followed

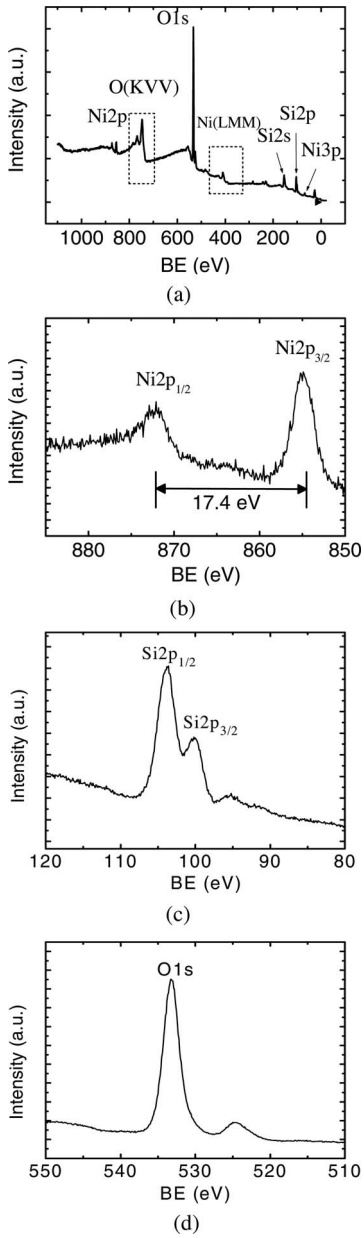

Fig. 3. (a) XPS survey spectrum of $NiSi_2$ NCs on a SiO_2/Si substrate, (b) high-resolution scan of the Ni 2p peaks, (c) high-resolution scan of the Si 2p peaks, and (d) high-resolution scan of O1s peak.

by 900 °C dopant activation annealing to obtain the heavily doped regions. Finally, aluminum was evaporated and patterned as the contact material. The device characterization was carried out by the Agilent 4155C semiconductor parameter analyzer to sense the threshold voltage and Agilent 81104A pulse/pattern generator to program/erase the device. The feature size of the device tested in this experiment is 1 μm × 1 μm.

III. Results and Discussion

Fig. 2(a) shows a scanning electron microscope (SEM) image of the synthesized $NiSi_2$ NCs on tunnel oxide before the growth of control oxide. The dot morphology is relatively uniform. Fig. 2(b) shows a transmission electron microscope (TEM) image of a reference sample under the same process conditions as

TABLE I
BINDING ENERGIES OF BULK NI, NI DEPOSITED ON SI (NI/SI), NISI FILM, $NiSi_2$ FILM, AND $NiSi_2$ NCS

Sample	Ni $2p_{3/2}$	Si $2p_{3/2}$
Ni (bulk)	853.0 eV [21]	
Ni/Si	853.1 eV [22]	99.4 eV [22]
NiSi (film)	853.7 eV [22]	99.7 eV [22]
$NiSi_2$ (film)	854.3 eV [22]	99.9 eV [22]
$NiSi_2$ (NCs) (this work)	855.0 eV	100.0 eV

the MOSFET memory sample except that the control oxide was adjusted to be slightly thicker, 30 nm, for TEM sampling. The average size of the $NiSi_2$ dots is about 7–10 nm, and they are homogeneous and well separated from each other. The density of the $NiSi_2$ NCs is determined to be $\sim 3 \times 10^{11}$ cm^{-2}. It should be noted that VSS (VLS) has intrinsic capability to achieve silicide NCs with much higher density $>10^{12}$ cm^{-2}, as seen from NW research [19], which is critical for future nonvolatile memory applications. We argue that this study serves as the first try of using VSS method to synthesize silicide NCs for memory applications; therefore, the dot density has not been optimized. The effort toward the density optimization is in progress.

X-ray photoelectron spectroscopy (XPS) was used to ascertain the chemical composition of the catalyst NCs. Spectra were collected from the NCs and from a NiSi film (as a standard) using Mg Kα radiation. All spectra were calibrated by assigning the O1s binding energy (BE) to 533.2 eV [20], [21]. A survey spectrum collected from the NCs of a reference sample before the control oxide was grown is shown in Fig. 3(a), and Fig. 3(b)–(d) shows the high-resolution spectra of the Ni 2p, Si 2p, and O1s levels, respectively. The Ni 2p3/2 and Si 2p3/2 BEs are given in Table I for the NCs along with values from the literature for Ni metal [22], Ni deposited on Si [23], and two stable silicides, NiSi and $NiSi_2$ [23]. The Ni 2p3/2 peak from $NiSi_2$ NCs locates at 855 eV, which is slightly higher than that from $NiSi_2$ film (854.3 eV) reported in [22]. The BE shift in $NiSi_2$ NCs is due to the reduction of screening in excess positive charge being distributed over the nanoparticle surface, increasing the core-level BE to a higher value [24], [25]. In addition, once the NC size is very small, the bandgap and BE increase as the size of the materials decreases [26]–[28]. We also performed XPS measurements on two reference samples (results are not shown here): one is $NiSi_2$ film formed by depositing and annealing a thin Ni film on a Si substrate, and the other is the Ni NCs formed by depositing a thin Ni film onto a SiO_2/Si substrate followed by annealing. The former was used to confirm that our silicide NCs are actually Ni disilicide and the latter was used for ruling out the possibility of silicide formation before VSS growth took place.

Fig. 4 shows the transfer characteristics (I_D–V_G) of the $NiSi_2$ NC MOSFET memory. FN mechanism, i.e., the gate voltage of $+18$ V for 1 s, was used to program the device. For erasing, the gate voltage of -18 V for 1 s was applied to erase the programmed device. A threshold voltage shift is clearly observed between programmed and erased states, indicating the charging/discharging effect of the electrons stored on $NiSi_2$ NCs. A memory window (V_T shift between programmed and erased states) of 1.51 V is obtained when using the industry standard of 100 nA drain current to define the threshold voltage. For the control device without NCs embedded, an insignificant threshold voltage shift ($<$0.1 V) was found at the same programming and erasing voltages, which confirms that the memory effect observed in $NiSi_2$ NC memory is dominated by the charging effect of the NCs, rather than by defect or interface states.

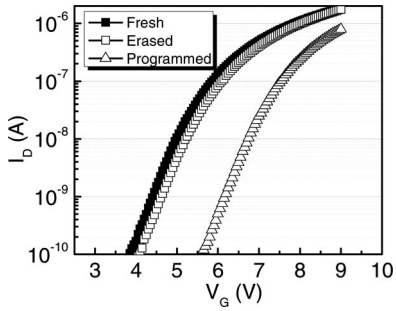

Fig. 4. Transfer characteristics of $NiSi_2$ NC MOSFET memory. Three I_D–V_G curves from left to right correspond to fresh, erased, and programmed states.

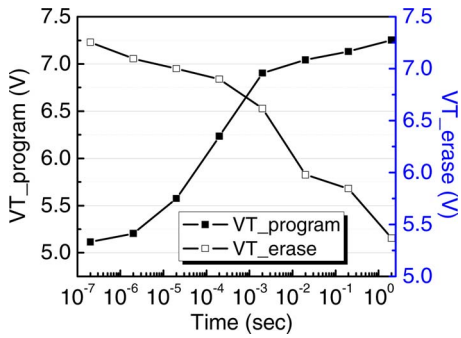

Fig. 5. Programming and erasing characteristics of $NiSi_2$ NC memory. Program and erase conditions are $V_G = 20$ V and $V_G = -20$ V, respectively.

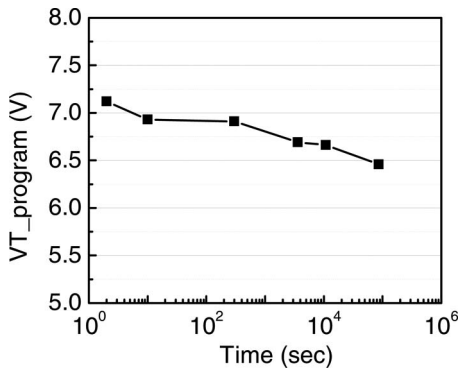

Fig. 6. Room temperature retention characteristics of FN programmed $NiSi_2$ NC memory.

Fig. 5 shows transient programming and erasing characteristics of $NiSi_2$ NC memory. The programming and erasing conditions are gate biases of ± 20 V, respectively. Before programming, the device was fully erased first by applying a gate bias of -20 V for 5 s. During programming, the threshold voltage shifts 1.68 V from the erased state after 1 ms, and after 1 s the shift increases to 2.2 V and the threshold voltage gets saturated. For erasing, the device was first programmed at $+20$ V for 5 s.

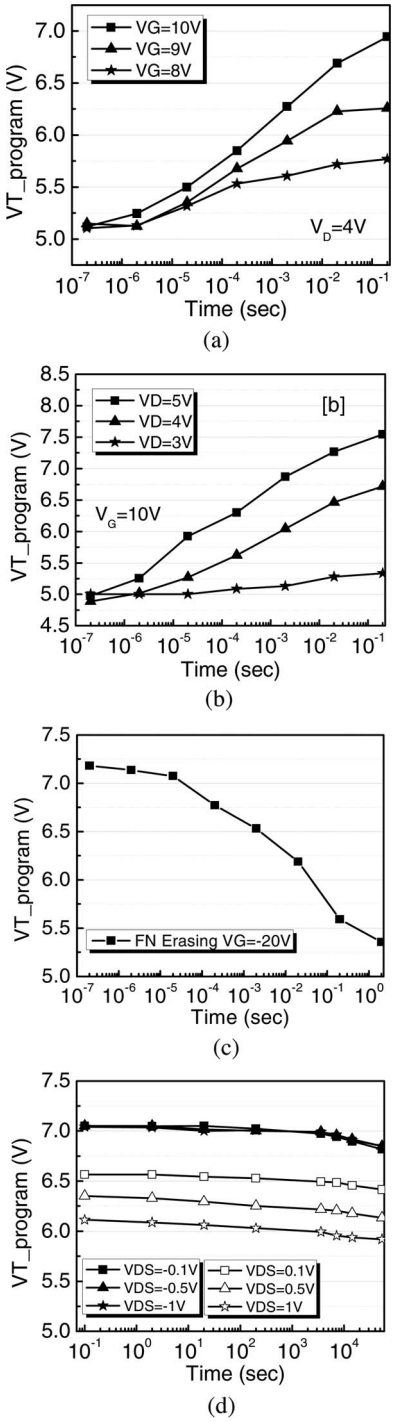

Fig. 7. (a) HCI transient programming characteristics under fixed drain voltage and various gate voltages, (b) HCI transient programming characteristics under fixed gate voltage and various drain voltages, (c) FN erasing characteristics with $V_G = -20$ V. The cell was programmed through HCI with $V_G/V_D = 10$ V/4 V, and (d) room temperature retention performances of HCI-programmed device under forward and reversed reading conditions.

As seen from Fig. 5, after 1 ms, the threshold voltage shifts 0.56 V toward the erased state, and after 2 s it shifts all the way back to the fully erased position.

Fig. 6 shows the retention characteristics of $NiSi_2$ NC memory device, which plots threshold voltage of FN-programmed device as a function of waiting time. The experiment was carried

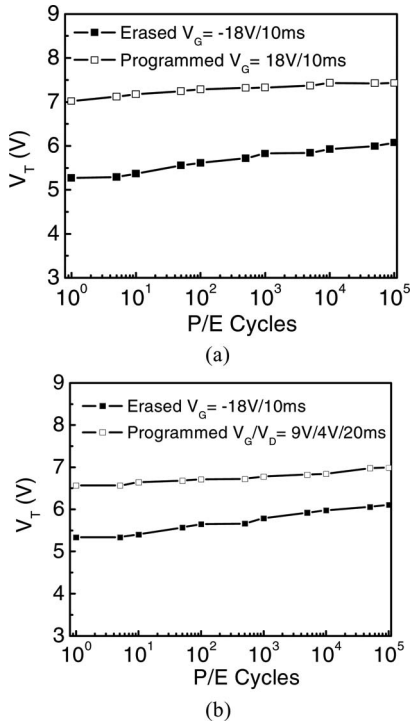

Fig. 8. Endurance performance of $NiSi_2$ NC memory under (a) FN operation mode and (b) HCI operation mode.

out at room temperature. The programming condition is $+20$ V for 5 s. The retention was recorded up to 10^5 s and the data trend suggests that the device has a good retention.

Fig. 7(a) and (b) shows the transient programming performances of $NiSi_2$ NC memory under HCI program scheme. HCI was performed by simultaneously biasing the gate and drain, leading to the injection of charges into floating gate around drain side. Fig. 7(a) shows the plot with V_D fixed and V_G changed from 8 to 10 V and Fig. 7(b) shows the plot with V_G fixed and V_D changed from 3 to 5 V. The program time accumulated from nanoseconds to seconds. Both gate and drain biases affect the charging efficiency, i.e., the higher the bias, the more the charge injected. This is reasonable as electrons gain higher energy at higher drain voltage and higher gate voltages attract more electrons from the channel to the floating gate. Fig.7(c) shows the erasing characteristics of an HCI-programmed device by biasing a negative gate voltage, while keeping source and drain floated and body contact common. The erasing curve shows similar trend to the one with FN operation shown in Fig. 5 except that the starting point to erase in this case is a partially charged cell while in the FN case, it is a fully and uniformly charged state. Fig. 7(d) shows the room temperature retention characteristics of an HCI-programmed device. Forward (read at the drain side) and reverse (read at the source side) readings at various read voltages were used. Due to the local charge storage around drain side, an additional energy barrier was formed for channel electrons. When reading from the drain side, the barrier was effectively lowered at large reading voltages, resulting in different V_T. On the other hand, when reading from the source side, the source voltage does not effectively change this barrier, leading

to insignificant change of V_T. This indicates the discrete nature of these NCs, leading to local charge storage for potential two-bit-per-cell applications. Similar to FN-programmed device, the HCI-programmed device also has a good retention performance judging from the threshold voltage shift.

Fig. 8(a) and (b) shows the device endurance performance under FN and HCI program schemes, respectively. The programming and erasing conditions are indicated in the figures. The memory window stays open at about 77% and 72% of the original window after 10^5 times of programming/erasing operation cycles under FN and HCI program schemes, respectively. This is an indication of good endurance performance. The slight up-shift of the threshold voltage is due to the electrons trapping into the defect levels in the oxide layer during the operations.

IV. Conclusion

$NiSi_2$ NCs were synthesized by VSS growth of Si into Ni catalysts in an LPCVD. MOSFET memory with $NiSi_2$ NCs as the floating gate was fabricated and characterized. Good memory performance, including fast programming/erasing, long retention time, and good endurance, was demonstrated. Due to superior thermal stability properties, $NiSi_2$ NCs formed by a simple VSS process may be promising in the future nonvolatile memory technologies. Further optimization of density, size, and uniformity of silicide NCs for nonvolatile memory is in progress.

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