Graphene based nickel nanocrystal flash memory

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Graphene based flash memory was demonstrated by using nickel nanocrystals as storage nodes. As-grown graphene films were characterized by transmission electron microscopy and Raman spectroscopy to show good film quality. On/off operation of the transistor memory was acquired by static pulse response measurement. The memory window of the device was found up to be 23.1 V by back gate sweep. This memory effect is attributed to charging/discharging of nanocrystals. Furthermore, excellent retention and endurance performance were achieved. © *2011 American Institute of Physics*. [doi:10.1063/1.3640210]

As a potential candidate to replace silicon for future nanoelectronics, graphene has been used to fabricate various devices such as inverters,[1] radio-frequency transistors,[2] spin transport devices,[3] resistive switches,[4,5] ferroelectric memory,[6] and flash memory.[7,8] Among these flash memories, water molecules or hydroxyl groups located on the interface between graphene and air were used as storage nodes.[7,8] The memory performance was strongly dependent on the surrounding air humidity and fabrication processes. For example, stored charges can easily leak out as a result of direct exposure of storage nodes to the ambient, leading to short retention performance of only several hours.[7] To resolve these issues, we propose a structure of graphene flash memory using embedded nickel (Ni) nanocrystals as storage layer. Figure 1 shows the schematic of the device. High performance is demonstrated.

To fabricate the device, graphene films were synthesized on Co thin films in a thermal cracker enhanced gas source molecule beam expitaxy and were then transferred onto a SiO_2(300 nm)/Si substrate. The growth details can be found elsewhere.[9] Figure 2(a) shows a planar view transmission electron microscopy (TEM) image of the graphene film. The even brightness of the film indicates a good morphology of the as-grown film. Most part of the film is comprised by single or bi-layer graphene as shown in the inset of Fig. 2(a), which can also be proved by the low intensity ratio of G peak and 2D peak (less than 1) in Raman spectrum (Fig. 2(b)).[10] The absence of D peak in the Raman curve and clear hexagonal diffraction pattern (Fig. 2(c)) indicate the high quality of as-grown film.

After the film was transferred onto the SiO_2/Si substrate, the sample was annealed at 450 °C for 2 h under H_2/Ar (100 sccm/100 sccm) flow to eliminate the surface adsorbates (such as water molecule) and polymethyl-methacrylate residue occurred during the transfer. Photolithography was then carried out to create a 20 μm × 5 μm pattern followed by the deposition of 50 nm Cr mask using an electron beam evaporator. Oxygen plasma process was then conducted to etch the unprotected area in a reactive ion etching system to make the graphene channel. A second photolithographic step was used to open windows at the two ends of the graphene channel, followed by the deposition of Ti/Au (10 nm/80 nm) into these windows to form source and drain contacts. The highly doped n-type Si substrate with a resistivity of 0.025–0.05 Ω·cm was directly used as back gate. After that, a 10 nm HfO_2 was grown at 110 °C on the top of the graphene channel by atomic layer deposition (ALD) to form the tunneling layer. A 1 nm Ni layer was then deposited on the HfO_2 film to form Ni nanocrystals (see supplementary materials for details[14]). Finally, another 30 nm HfO_2 blocking oxide was grown by ALD to passivate the nanocrystals. Since the source/drain metals were also covered by the deposited HfO_2 film, a third photolithography step was conducted to open windows at the source/drain areas, where the insulator film was etched by a HF solution until the metal contacts were exposed.

Fig. 3(a) shows the change in drain current I_d with the back gate sweep within a ±20 V range. The Dirac point shift, i.e., memory window of larger than 10 V was demonstrated, which is much bigger than other reported graphene or carbon nanotube flash memory data.[7,11] The reason that the device can be programmed and erased with a back gate is that unlike a planar two-dimensional Si channel, the graphene strip here can be considered as one-dimensional channel because of its much smaller size compared to the two-dimensional back gate. In this case, the fringing electric fields originated from the gate have effect on both the channel and the nanocrystals. Therefore, the nanocrystals have a potential between that of the back gate and the channel, which is grounded during the programming/erasing, and the potential difference between the nanocrystals and channel results in charging and discharging of the storage node

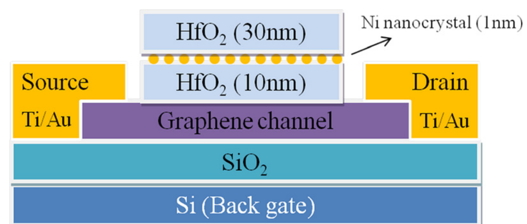

FIG. 1. (Color online) Schematic of graphene channeled Ni nanocrystal flash memory.

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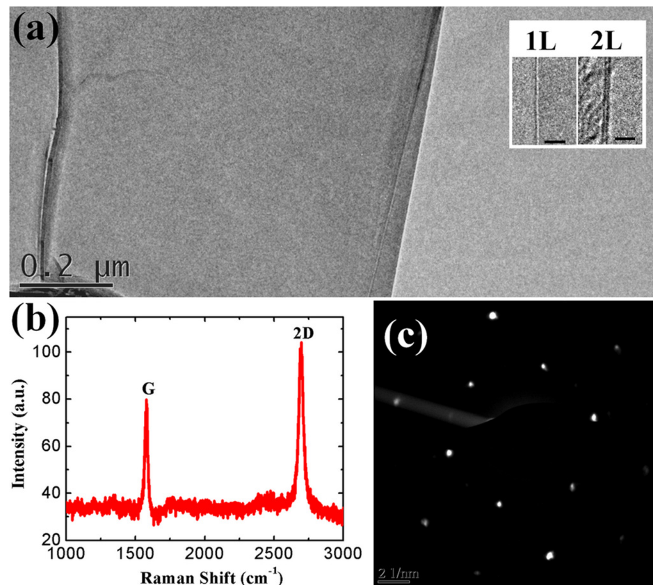

FIG. 2. (Color online) (a) Top-view TEM image of the graphene film. The inset shows the cross-sectional images of single and bi-layer graphene, respectively (the scale bar is 2 nm). (b) Raman spectrum of synthesized graphene film. (c) Diffraction pattern of as-grown sample.

during the operation.[12] As seen in Fig. 3(a), when the sweep starts with −20 V, electrons are repelled from the nanocrystals through the oxide to the graphene, which moves the Dirac point to the left. As the sweep starts from +20 V, the Dirac point is shifted to the right due to the electron storage from the channel to the nanocrystals.

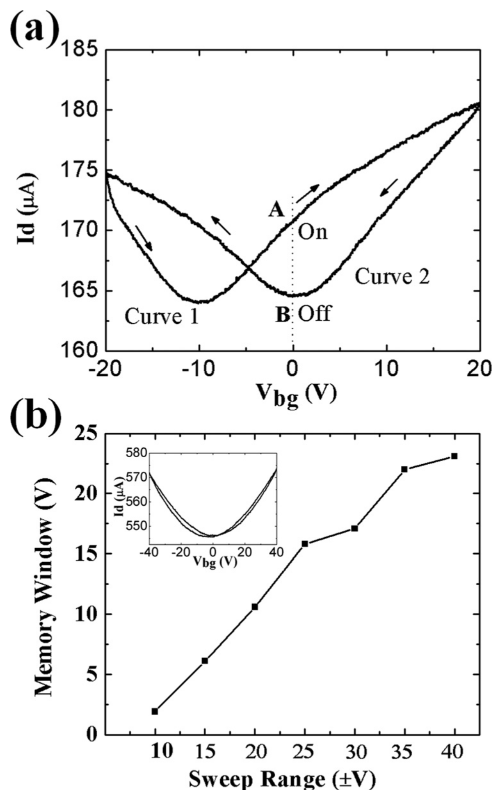

FIG. 3. (a) Transfer curves of graphene based Ni nanocrystal memory at the drain voltage V_{ds} of 1 V. The gate sweep direction is indicated by the arrows. (b) Memory window as a function of the sweep range for graphene based Ni nanocrystal memory. The inset shows the $I_d - V_{bg}$ sweep for the reference device without Ni nanocrystals.

Figure 3(b) shows memory windows at different sweep ranges. The memory window is only 1.9 V when the range is from −10 V to +10 V and increases almost linearly with the increase of the range from ±10 V to ±35 V, beyond which it starts to show saturation. The window reaches 23.1 V when the range is ±40 V. To clarify the source of this memory effect, a reference device was also fabricated. Only 40 nm HfO_2 cap layer was deposited on graphene channel with the same recipe by ALD, and no Ni nanocrystal was embedded in HfO_2 thin film. The inset of Fig. 3(b) shows the transfer curves for this reference device. Only a small memory window of about 3 V was found compared to that of 23.1 V for the nanocrystal device under similar sweep range. As mentioned before, the only difference between the nanocrystal device and the reference sample is the embedded Ni nanocrystals, indicating that the large memory window primarily derives from the Ni nanocrystals but not the HfO_2 thin film. However, the small memory window of the reference sample should be due to the existence of bulk traps in HfO_2.[13]

To further study the memory effect of the device, bipolar pulse signals of ±20 V were applied on the back gate as program/erase biases. The reading gate bias was set to 0 V to eliminate the static charge and its effect on retention performance during testing (Fig. 4(a)). The very short pulse with width of 10 ms periodically charges or discharges the nanocrystals and shifts the $I_d - V_{bg}$ scan. After a positive gate pulse, the Dirac point shifts right as shown by curve 2 in Fig. 3(a), while curve 1 is a result of a negative gate pulse. To understand the on/off operation of this device, the higher current (point A) at zero gate bias in curve 1 is defined as on state, and the lower point B in curve 2 is recognized as off state in Fig. 3(a). During static pulse response measurement,

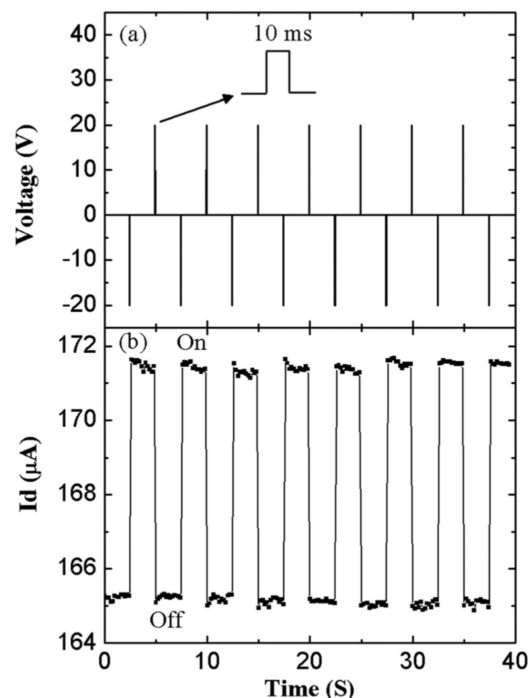

FIG. 4. Memory effect of graphene based Ni nanocrystal memory. (a) A back gate trigger signal with amplitudes of ±20 V, a pulse width of 10 ms, and a period of 5 s. (b) Drain current response to the trigger signal in (a).

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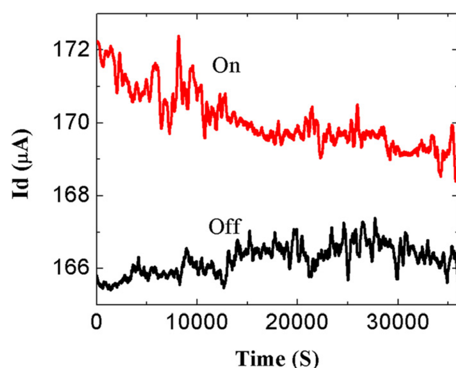

FIG. 5. (Color online) Retention performance for the on and off states of graphene based Ni nanocrystal memory.

as shown in Fig. 4(b), the on and off states, which were monitored under the drain voltage of 1 V, appear immediately after a negative or positive 20 V pulse. The two states persist after the pulse is reset, which indicates the good memory performance of the device. Additionally, endurance testing was done with the same ±20 V pulse on the back gate at a frequency of 5 Hz and a duty cycle of 0.2%. No obvious failure or performance degradation was found after programming/erasing cycles of 5×10^5, which suggests very good endurance of the device. While the same bipolar pulse was applied on the reference sample, no distinguishable on and off states were found (not shown here), which indicates little memory effect for the reference sample.

Because of a relatively flatten curve near the Dirac point in the ambipolar transfer characteristic, drain current instead of threshold voltage change versus time has been chosen to perform retention test for the device. A +20 V/−20 V bias was applied on the back gate for 10 s prior to the off state/on state retention test, respectively. Figure 5 shows the on and off states retention performance while the drain is constantly biased at 1 V. Both on and off state currents decay slightly during the earlier retention stage within about 1.4×10^4 s, after which an evidently large memory window was still observed even if the measurement reaches 3.6×10^4 s, indicating significant improved charge retention performance over other graphene or carbon nanotube flash memory devices.[7,11] The improvement attributes to much better charge retention ability of embedded Ni nanocrystals compared to that of water molecules[7] and bulk oxide defects.[11]

In summary, Ni nanocrystals were used as storage node for graphene field effect transistor memory. Large memory window of 23.1 V was demonstrated. Excellent endurance and long retention were also observed. The results suggest that nanocrystal based graphene memory is promising for future nonvolatile memory technologies.

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[14]See supplementary material at http://dx.doi.org/10.1063/1.3640210 for synthesis and characterization of Ni nanocrystals.

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