# $TiSi_2$ Nanocrystal Metal Oxide Semiconductor Field Effect Transistor Memory

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***Abstract*—A $TiSi_2$ nanocrystal (NC) memory was fabricated. $TiSi_2$ NCs were synthesized on $SiO_2$ by annealing Ti covered Si NCs. Compared to the reference Si NC memory, both experiment and simulation results show that $TiSi_2$ NC memory exhibits larger memory window, faster writing and erasing, and longer retention lifetime as a result of the metallic property of the silicide NCs. Due to thermally stable, CMOS compatible properties, $TiSi_2$ NCs are highly promising for nonvolatile memory device application.**

***Index Terms*—Nonvolatile memory (NVM), $TiSi_2$ nanocrystal (NC).**

## I. Introduction

POLYCRYSTALLINE silicon as a floating gate has been used as a charge storage material in nonvolatile memory (NVM) for the past three decades [1]. The dimensions of Si-based memory devices have approached the nanometer scale and NVM, utilizing discrete charge storage nodes such as defect traps and Si nanocrystals (NCs) has been considered as a candidate to replace the conventional flash memory [2], [3]. It was also reported that the wide distribution of defect-related deep levels are associated with the Si NC memory [4]. Although the existence of these defects in Si NCs results in relatively long retention performance, the defect-based performance improvement is not stable in the subsequent high-temperature annealing step of MOSFET memory device fabrication [4].

New types of NC floating dots such as double Si dots [5], Ge NCs [6], metal [7]–[10] or metal-like [11] dots, and dielectric NCs ($Al_2O_3$, $HfO_2$, and $Si_3N_4$, etc.) [12]–[14], have been proposed to achieve memory devices with longer retention performance. Metal NCs are the perfect material to be used as a floating gate to improve the programming speed [15]–[17]. However, the drawback of using metal NCs is the interdiffusion between NCs and tunnel oxide during device integration, which degrades the tunnel oxide and worsens retention performance [18]–[20]. Since post annealing is necessary for most of the device process, the thermal stability of such a memory cell has become an issue. In this study, we propose and experimentally verify a method to improve the thermal stability of the memory cell by using self-aligned $TiSi_2$ NCs.

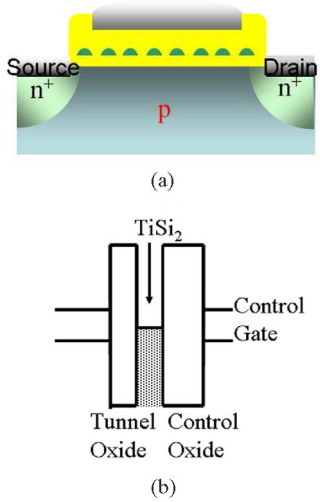


Fig. 1. (a) Schematic cross section of $TiSi_2$ NC memory device. (b) Energy band diagram for $TiSi_2$ NC memory.

Fig. 1(a) and (b) shows the cross section schematic and energy band diagram of a $TiSi_2$ NC memory, respectively. The wide distribution of defect-related deep levels in the forbidden gap of Si associated with Si NC memory reported in [4], [21], and [22] leads to easy loss of charges during the retention. In contrast, the Fermi level of $TiSi_2$ is within the bandgap of Si and 0.6 eV below the conduction bandedge of Si [23], as shown in Fig. 1(b), which significantly prolongs the charge retention. Metallic $TiSi_2$ NCs not only make the devices more stable in the high-temperature annealing process during the device fabrication, but also improve the programming speed of the devices, which is proven by the following experiments and simulations.

## II. Experiment

The $TiSi_2$ NC fabrication process begins with a thermal oxide deposition of about 5 nm, which was grown at 850 °C. Si NCs

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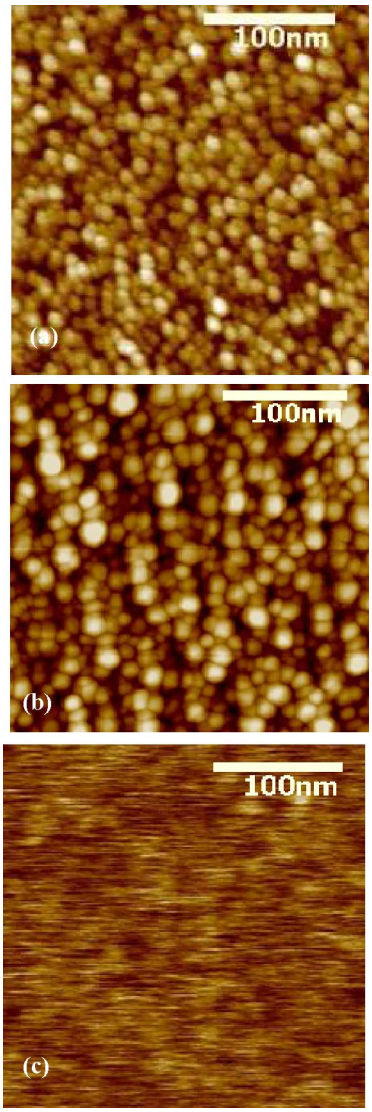


Fig. 2. AFM images for (a) Si NCs, (b) as-fabricated $TiSi_2$ NCs, and (c) $TiSi_2$ NCs after diluted hydrofluoric acid etching.

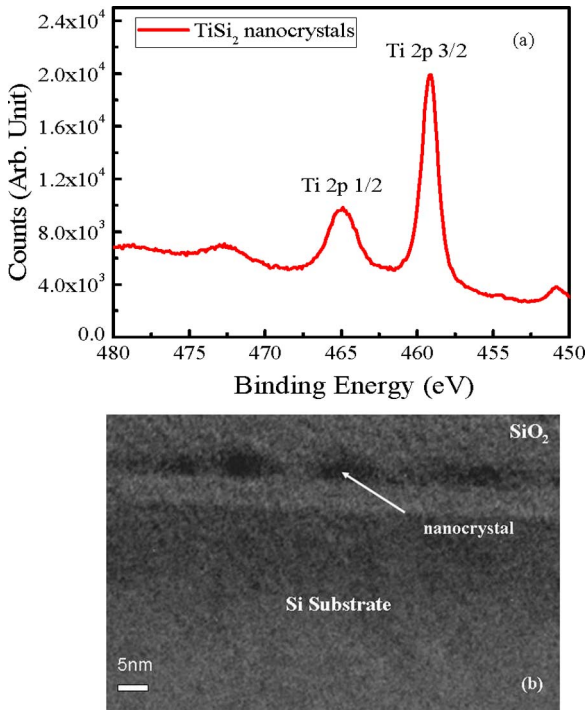


Fig. 3. (a) XPS for as-fabricated $TiSi_2$ NCs. (b) TEM image for $TiSi_2$ NCs.

were grown at 610 °C for 15 s with the pressure of 400 mtorr in a low-pressure chemical vapor deposition (CVD) system. $TiSi_2$ NCs were fabricated with a two-step-annealing silicidation method. First a 10-nm-thick metal Ti layer was deposited onto the sample. Then, the first annealing was performed in nitrogen at 775 °C for 60 s. The unreacted Ti metal on top of NCs as well as in between NCs was removed in selective etchant $NH_4OH{:}H_2O_2{:}H_2O = 1{:}1{:}5$. The second annealing was performed at 880 °C for 30 s after the metal removal to form more thermally robust $TiSi_2$ dots. The sample was then capped with control oxide of about 15 nm in a low-temperature oxide CVD furnace. Standard MOSFET process was performed afterward to form MOSFET memory devices.

Fig. 2(a)–(c) shows the atomic force microscope (AFM) images of the reference Si NCs, subsequently prepared silicide NCs, and a silicide NC sample after diluted HF etching, respectively. Both Si NC density and silicide NC density are about $5 \times 10^{11}$ $cm^{-2}$, suggesting excellent self-aligned formation of silicide dots from Si dots. The smooth substrate surface shown in Fig. 2(c) indicates that all the silicide NCs were removed by diluted HF. This experiment confirms that all original Si NCs have been converted to silicide NCs during the annealing process. Therefore, these NCs are different with our $TiSi_2$/Si heteronanocrystals reported earlier [24]. Further improvement includes more energy levels available in pure silicide NCs over heteronanocrystals, leading to wider memory window and faster programming/erasing speeds. Fig. 3(a) shows the result of X-ray photoelectron spectroscopy (XPS) measurement for the silicide NC sample. One evident peak at ∼460 eV is corresponding to Ti 2P3/2 states of $TiSi_2$. The combination of AFM and XPS results suggests that $TiSi_2$ NCs have been achieved. Fig. 3(b) shows a typical cross-sectional transmission electron microscope (TEM) image of a dedicated $TiSi_2$ NC device sample. The NCs are of approximate dome shapes. Based on the average of a group of TEM images, the width of NCs are approximately determined to be ∼7 nm. The average distance between the NCs is ∼5 nm. These values are close to the AFM results, considering the tip effect. The thickness of the tunnel oxide is ∼5 nm and the control oxide is also estimated from these TEM measurements to be ∼15 nm, both of which are designed values and consistent with our ellipsometry measurements.

Si NC and $TiSi_2$ NC memories were fabricated and characterized. Fig. 4(a) shows typical high-frequency (1 MHz) capacitance–voltage ($C$–$V$) sweep results for $TiSi_2$ NC and Si NC MOS capacitor memories with scanning range between −15 and +15 V. The sweep began from inversion region to accumulation region and back to inversion region again. The voltage sweep rate is 0.5 V/s. It is found that $C$–$V$ curves exhibit evident hysteresis with a voltage shift of around 3.1 V for $TiSi_2$

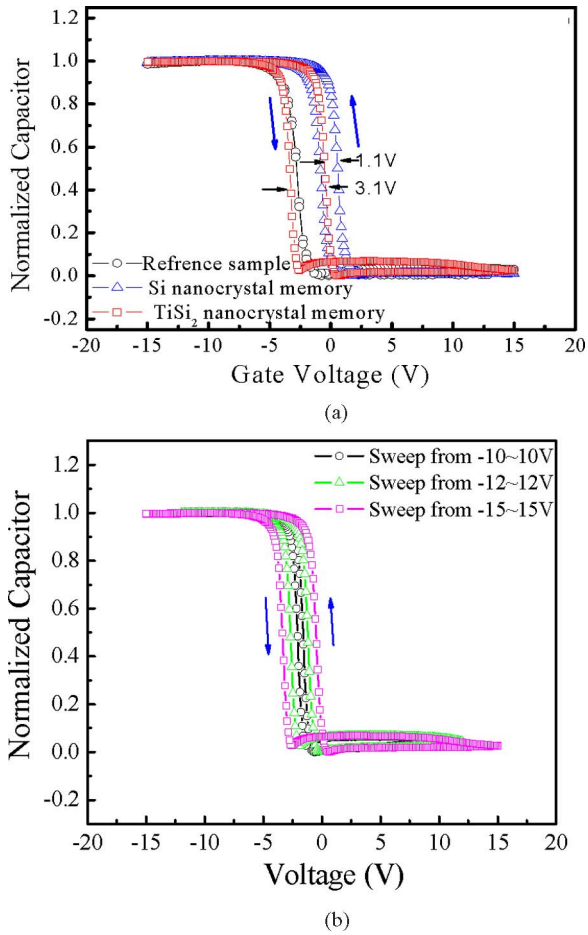


Fig. 4. (a) *C–V* sweep measurement for the $TiSi_2$ NC MOS memory and Si NC MOS memory capacitor. (b) *C–V* hysteresis of $TiSi_2$ NC MOS memory capacitor after sweeps between 10 V (−10 V), 12 V (−12 V), and 15 V (−15 V), The size for the capacitor is 400 $\mu$m × 400 $\mu$m.

NC memory and 1.1 V for Si NC memory, indicating that $TiSi_2$ NC memory shows stronger memory effects than that of the Si NC memory. Fig. 4(b) shows the bidirectional *C–V* sweeps with different scanning range from ±10 to ±15 V for $TiSi_2$ NC MOS capacitor memory. When voltage sweeps from 10 to −10 V and back to 10 V, a very small flatband voltage shift is observed. When the sweep voltage increases to 12 and 15 V, the flat band voltage shift shows larger memory window at 1.5 and 3.1 V, respectively. Wider voltage sweep range leads to the fact that more electrons are written/erased from the $TiSi_2$ NCs, therefore, larger memory window is achieved.

Fig. 5 shows the source–drain current ($I_{\rm ds}$) as a function of gate voltage ($V_g$) for $TiSi_2$ NC MOSFET memory in the neutral state and writing state, which was characterized with an Agilent 4155 A semiconductor analyzer and Agilent 81104 A Pulse Generator at room temperature. The programming was performed at 15 V for 100 ms. The shift of the *I–V* curve toward higher gate voltage indicates the electron storage in the NCs.

Fig. 6(a) shows the threshold voltage shift ($\Delta V_{\rm th}$) as a function of writing time in both $TiSi_2$ NC and reference Si NC MOSFET memory devices. It is evident that $\Delta V_{\rm th}$ increases with writing time until it finally saturates. This is due to the fact

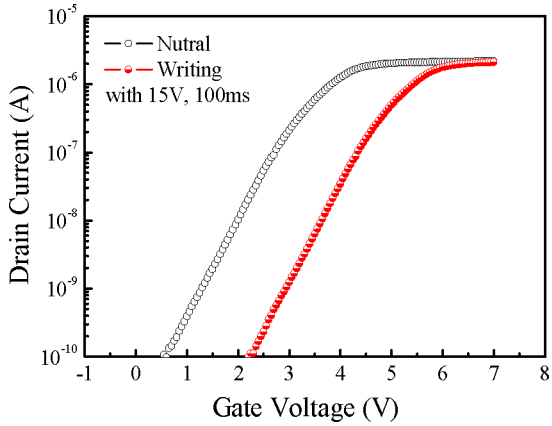


Fig. 5. Memory effect from a $TiSi_2$ NC MOSFET memory cell. The shift of $I_{\rm ds}$–$V_g$ curve after writing operation indicates the electron storage in the floating gate. The channel length of the device is 1$\mu$m.

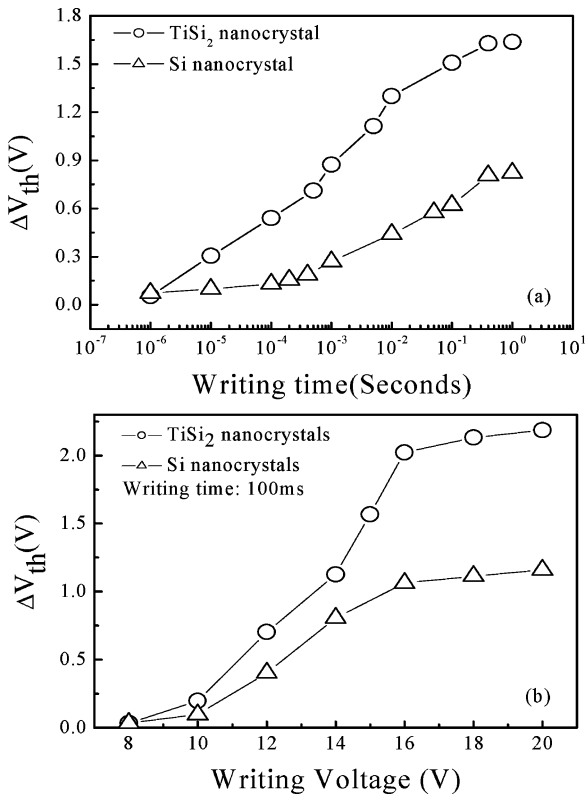


Fig. 6. $\Delta V_{\rm th}$ as a function of (a) writing time at a fixed writing voltage of 15 V and (b) writing voltage at a fixed writing time of 100 ms, for MOSFET memory cells with $TiSi_2$ NCs and reference Si NCs, respectively.

that as the writing time increases, more and more electrons are injected into the NCs until they are unable to accept more electrons. Fig. 6(b) shows the dependence of $\Delta V_{\rm th}$ on the writing voltage in $TiSi_2$ NC and reference Si NC memory devices. At the beginning, the writing voltage is not high enough to make the electrons go through the tunneling oxide by Fowler–Nordheim (F–N) tunneling and almost no electrons are injected to the NCs, therefore, almost no threshold voltage shift was observed. As the writing voltage increases, the edge of the conduction band of tunneling oxide becomes triangular shaped and the slope of the

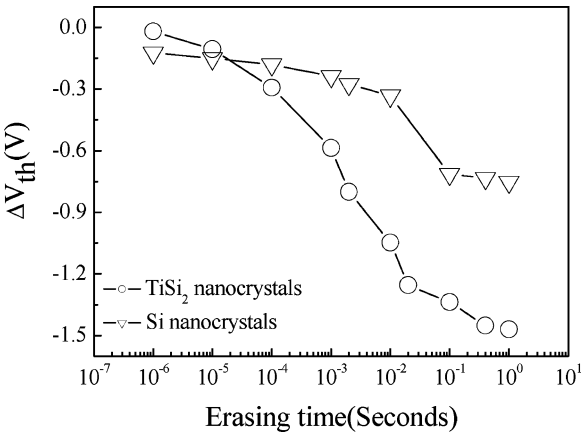


Fig. 7. $\Delta V_{\rm th}$ as a function of erasing time for MOSFET memory cells with $TiSi_2$ NCs and reference Si NCs, respectively.

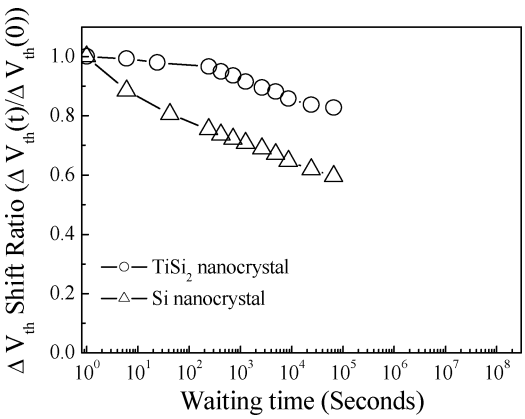


Fig. 8. Retention performance comparison between reference Si NC MOSFET device and $TiSi_2$ NC MOSFET memory device. The writing was done at 20 V for 1 s.

triangle increases, which allows the electrons in the Si substrate to go through the tunneling oxide layer by F–N tunneling and reach the NCs. As the writing voltage reaches ~15 V or more, the device $\Delta V_{\rm th}$ saturates and the saturation voltage is around 2 V. We further calculate the electron storage in terms of their threshold voltage shifting, which is defined as [25],

$$\Delta V_{\rm th} = \frac{Q_{\rm ox} T_{\rm cox}}{\varepsilon_{\rm ox}} \tag{1}$$

where $\varepsilon_{\rm ox}$ is the dielectric constant of $SiO_2$ and $T_{\rm cox}$ the thickness of control oxide. The electrons storage at the saturation is estimated to be six electrons per $TiSi_2$ dot.

The change in threshold voltage as a function of erasing time is shown in Fig. 7. The magnitude of $\Delta V_{\rm th}$ increases as the erasing time increases in both $TiSi_2$ NC memory and Si NC memory. In the $TiSi_2$ NC memory, because of higher density of state (DOS) than that of Si NCs, more electrons are available to be erased, which makes the $\Delta V_{\rm th}$ saturate at a higher value than Si NC memory device.

The retention characteristics are shown in Fig. 8 for the two devices with $TiSi_2$ NCs and Si NCs, respectively. The devices were programmed at 20 V for 1 s. $TiSi_2$ NCs lead to slower charge loss rate because of its lower occupied energy levels in the NCs. Electrons in the $TiSi_2$ NCs occupy the low energy level and are more difficult to tunnel through the tunneling oxide layer than electrons in Si NCs. Therefore, the $TiSi_2$ NC memory device shows better retention performance than reference Si NC memory device.

## III. Simulation

To clarify the physical mechanism in the writing and erasing process of $TiSi_2$ NC memory device, Schrodinger equation and Poisson–Boltzmann's equation are combined to calculate the energy band distribution in writing and erasing process by self-consistent calculation in 1-D [26], [27]. It should be noted that 1-D simulation can provide straightforward and relatively accurate answers to this problem; more accurate results may be obtained through 3-D simulations [28], [29].

The electrical potential $\phi$ (with respect to the substrate potential) satisfies the Poisson–Boltzmann's equation

$$\frac{d}{dx}\left(\varepsilon \frac{d}{dx}\phi\right) = q(p - n + D) \tag{2}$$

where $q$ is the elementary electron charge, $\varepsilon$ is the material permittivity, $n$ and $p$ are the mobile electron and hole densities, respectively, and $D$ is the concentration of ionized impurities (p-type doping).

The electron density in the NC is determined by the Schrodinger's equation

$$-\frac{\hbar^2}{2}\frac{d}{dx}\left(\frac{1}{m}\frac{d}{dx}u(x)\right) + V(x)u(x) = Eu(x) \tag{3}$$

where $u$, $E$, $V$, and  are the wave function, eigenenergy, potential energy, and reduced Planck's constant, respectively. The parameters for the devices are similar as those in real devices with 8 nm NC size, 5-nm tunneling oxide, 15-nm control oxide, and the calculation stops when maximum difference between successive potential distributions is 1mV.

Fig. 9(a) and (b) shows the conduction band edges for the two devices with the embedded $TiSi_2$ NCs and Si NCs in the writing and erasing biases, respectively. In Fig. 9(a), when 20 V is applied on the control gate, the edge of the conduction band in the tunneling oxide region and control oxide region shows a triangle shape. In the Si NC region, the edge of the conduction band also shows a triangular shape, indicating that the electric field penetrates the Si naocrystals and a certain amount of voltage drops on them. In the $TiSi_2$ NC structure, $TiSi_2$ is metallic. When the voltage is applied on the control gate, the electric field is screened at the surface, almost no voltage is dropped in the $TiSi_2$ NC region. Since the total voltage drop is the same for both devices, the electric field in the tunneling oxide is higher in the $TiSi_2$ NC memory than in the Si NC memory for a given applied voltage. The higher electric field in the tunneling oxide region increases the F–N tunneling of electrons from the Si substrate into the $TiSi_2$ NC compared to that of the Si NC during the writing phase.

The same effect occurs during the erasing process as shown by the conduction band edges plotted in Fig. 9(b). In the $TiSi_2$ NC memory, more voltage drops across the oxide layer compared

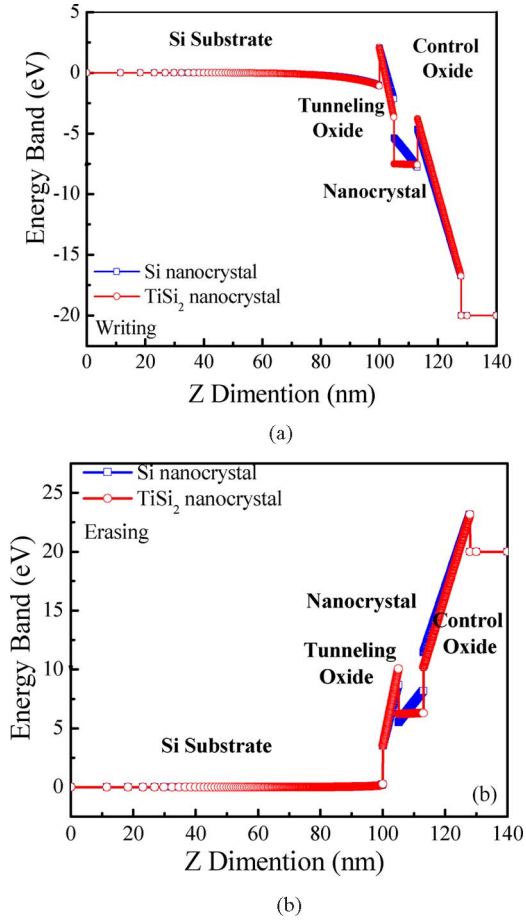


Fig. 9. Edge of conduction band distribution of $TiSi_2$ NC and reference Si NC devices in writing and erasing states (writing/erasing voltage is 20 V/−20 V). $\varepsilon$ is taken as 500 and 12 in $TiSi_2$ NC and Si NC respectively.

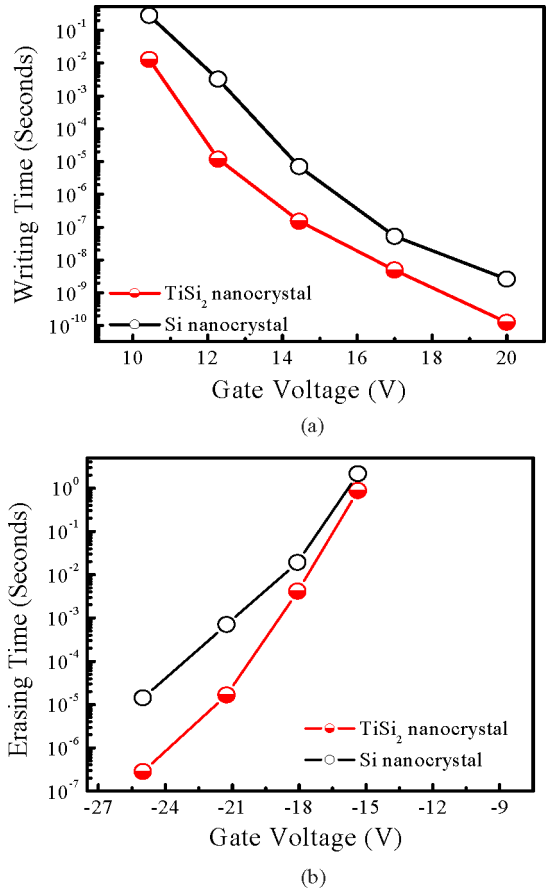


Fig. 10. Simulated programming speed versus operation voltage. (a) Writing time as a function of gate voltage. (b) Erasing time as a function of gate voltage. The shift of conduction band between Si and $SiO_2$ is set to be 3.1 eV.

to that of the Si NC memory. Thus, for a given voltage, the tunneling rate out of the NC into the Si is larger for the $TiSi_2$ NCs compared to that of the Si NCs.

The higher DOSs in the metallic $TiSi_2$ NC compared to that in the Si NC combined with the increased electric field in the tunneling oxide explains the difference in the reading and writing properties of the two different systems. During writing, before saturation, the increased electric field in the tunneling oxide of the $TiSi_2$ NCs gives rise to a larger $\Delta V_{\rm th}$ for a given voltage or time as shown in Fig. 6(a) and (b). The larger DOS of the $TiSi_2$ compared to that of the Si NCs results in a larger saturation value of $\Delta V_{\rm th}$ for the $TiSi_2$ NC structures as shown in Fig. 6(b). The larger electric field in the tunneling oxide also explains the larger $\Delta V_{\rm th}$ as a function of erase time for the $TiSi_2$ NC structures compared to that of the Si NC structures as seen in Fig. 7, although the reason for the crossover at very short times is not clear. Thus, overall, the improvement in performance of the $TiSi_2$ NC memory compared to the Si NC memory is consistent with an explanation based on 1) the different electric fields in the tunneling oxides resulting from the different screening properties of the NCs and 2) the different DOSs of the NCs.

The writing and erasing tunneling current densities are calculated using the method proposed in [30], considering the quantization of carriers in the inversion layer or the accumulation layer when the device is biased

$$J = q \int T(E) f(E) \rho(E) F(E) dE \tag{4}$$

where $f(E)$ is the impact frequency, $\rho(E)$ is the 2-D DOSs, $F(E)$ is the Fermi–Dirac distribution function, and $T(E)$ is the tunneling probability, respectively. The time concept in a memory device can be defined as the inverse of the tunneling current density [31]. The time $\tau$ is presented as

$$\tau = \frac{q}{J \times L^2} \tag{5}$$

where $q$, $J$, and $L$ are the electron charge, tunneling current density, and size of the NC, respectively.

Using (4) and (5), the calculated voltage dependences of the writing and erasing processes are shown in Fig. 10(a) and (b), respectively. It is found that, for both writing and erasing processes, the programming speed increases with the gate voltage. This is due to the change of the shape of the electron barrier in tunneling oxide region with the gate voltage. As the gate voltage increases, the electric field in tunneling oxide increases, which makes the electrons easier to go through the tunneling oxide. Since the electric field in tunneling oxide of $TiSi_2$ NC memory

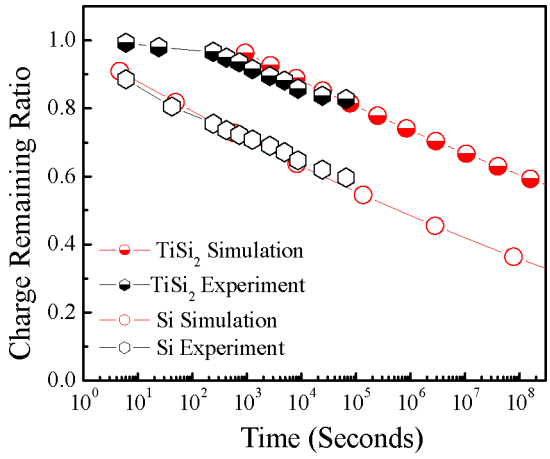


Fig. 11. Simulated retention performance of reference Si NC and $TiSi_2$ NC memory. To match with experiment result, $\phi_t$ is set to be 0.5eV for Si NC and 0.6 eV for $TiSi_2$ NC system.

is always larger than that in Si NC memory, $TiSi_2$ NC device shows faster programming speed than Si NC device.

To explain the retention characteristics, the trap-assisted tunneling mechanism is assumed. The retention time of the charge storage is calculated by Poole–Frenkel effect [32]. The leakage current is derived with the following method:

$$J = C_3 E \exp\left(-\frac{q\phi_t}{kT}\right) \exp\left(\frac{1}{\gamma kT}\sqrt{\frac{q^3}{\pi\varepsilon}E}\right) \quad (6)$$

where $\phi_t$ is trapped electrons' energy level below the dielectric conduction band and $r$ is the refractive index of dielectric films. $C_3$ relates to the trap density. Fig. 11 shows the retention performance comparison between the $TiSi_2$ NC memory and Si NC memory. The hollow symbol curves show the retention performance for Si NC memory and the solid symbol curves show the retention performance for $TiSi_2$ NC memory. The black color curves show the retention performance from experiment, which is also shown in Fig. 8. To match the real device, the potential is set to be 0 V on the control gate and the electric field in the tunneling oxide layer caused by the storage of electrons is calculated by Poisson equation. It is found that $TiSi_2$ NC memory device shows slower charge loss rate and higher charge storage after ten years, which is similar with the experimental result. $TiSi_2$ NCs store more electrons than Si NCs; moreover, the charge loss is slower due to the deeper well. These result in more electrons left in the NCs after ten years.

## IV. Conclusion

In summary, we fabricated $TiSi_2$ NC memories by two-step annealing process. Compared with the reference Si NC memory, $TiSi_2$ NC memory shows larger memory window, faster writing, erasing speed, and better retention performance. Schrodinger equation and Poisson–Boltzmann's equation are combined to do self-consistent calculation to clarify the physical mechanism. Metallic $TiSi_2$ NC-embedded memory shows higher electric field in tunneling oxide region leading to easier F–N tunneling, which explains faster writing and erasing performance in $TiSi_2$ NC memory. $TiSi_2$ NC memory also shows better retention performance in the calculation, which matches the real device characterization.

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