Nonvolatile Memory With Ge/Si Heteronanocrystals as Floating Gate

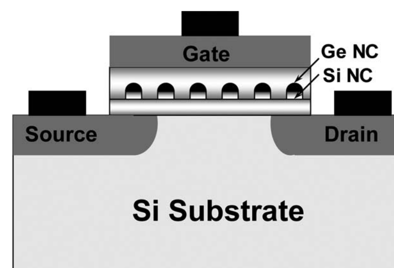
Bei Li and Jianlin Liu, *Member, IEEE*

***Abstract*—A p-channel memory with Ge/Si heteronanocrystals (HNCs) as the floating gate was fabricated and tested. The nanocrystals (NCs) were synthesized by low-pressure chemical vapor deposition of Si NCs followed by selective growth of Ge on top of Si. Both hole and electron storages were characterized in Ge/Si HNC memory. Fowler–Nordheim and hot carrier injection programming operations were studied. Compared to Si NC memory, enhanced memory performances were demonstrated in Ge/Si HNC memory in terms of longer retention, larger storage capability, and faster programming.**

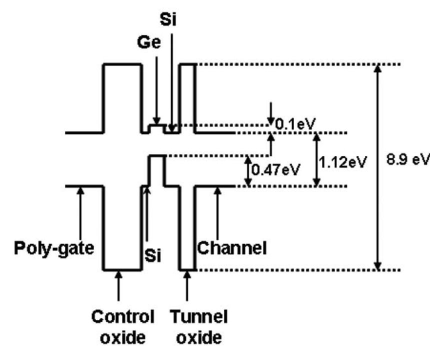
***Index Terms*—Ge/Si self-assembly, MOSFET, nanocrystal (NC) memory.**

I. Introduction

Nanocrystal (NC) memory as one of the most promising candidates to replace the conventional floating gate memory was introduced by Tiwari [1], [2] due to its potential to achieve low-power consumption, fast operation speed, and high scalability. For nonvolatile memory, tunnel oxide thickness is the most critical issue in device scaling. Compared to conventional flash memory, NC memory can use thinner tunnel oxide because the charge loss through lateral paths can be suppressed by localizing the charge into electrically discrete nodes. Once the tunnel oxide thickness shrinks, the programming/erasing speed is enhanced and the power to operate the device is reduced. Many NC memories have been developed and investigated, such as Si [3]–[5], Ge [6]–[8], silicide [9], [10], and metal NCs [11], [12]. In addition, high-κ dielectrics were introduced in NC memory to shrink the equivalent tunnel oxide thickness and reduce the interpoly leakage current [13]. Recently, we reported the fabrication of Ge/Si heteronanocrystals (HNCs) and their applications in nonvolatile memories [14]. The goal was to further improve the retention performance achieved in Si NC memory, without compromising the programming efficiency. The enhanced retention performance in Ge/Si HNC memory can be attributed to the type II band alignment between Si and Ge. As shown in Fig. 1(b), the valance band offset of 0.47 eV between Ge and Si makes it possible to localize the hole carriers, used for p-channel devices, mainly into Ge quantum well



(a)



(b)

Fig. 1. (a) Schematic cross section and (b) flat band energy diagram of Ge/Si HNC memory device.

so that a longer retention time is expected from the double barriers (Si NC and tunnel oxide) during retention and a thinner tunnel oxide can be used to obtain a faster operation speed. Therefore, the tradeoff between long retention time and fast operation speed can be solved by this artificially created quantum well. Simulation works [15]–[17] have been done showing the better performance of Ge/Si HNC memory compared to Si NC memory in terms of retention. Other stacked nanostructures have also been reported to solve the tradeoff between retention and programming, such as double layer of NC [18] and HNCs (silicide/Si) [19], where the combination of materials with different band gaps causes the injected carriers well stored in the side with lower band energy. The aim of this paper is to present a systematic characterization of Ge/Si HNC capacitors, MOSFET memories, including both electron and hole storages under Fowler–Nordheim (FN) and hot carrier injection (HCI) operations, which cannot be done in the original short report [14]. The results further support the fact that Ge/Si HNCs are superior to Si NCs for nonvolatile memory applications.

II. Device Fabrication

p-MOSFET processes were used to fabricate the Ge/Si HNC memory. Two reference devices (Si NC memory device and a

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The authors are with the Department of Electrical Engineering, University of California, Riverside, CA 92521 USA (e-mail: jianlin@ee.ucr.edu).

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MOSFET device without NC embedded) were fabricated simultaneously using the same processes as Ge/Si HNC memory for comparison. The device fabrication began with an n-Si (100). Local oxidation of silicon (LOCOS) process was used to electrically isolate devices. Field oxide and nitride were grown and deposited sequentially followed by photolithography and reactive ion etching (RIE) to define and expose the active region. Prediffusion cleaning was carried out followed by a 5 nm tunnel oxide growth at 850 °C and *in situ* annealing in N_2 at 900 °C. The thin nitride layer formed on tunnel oxide acts as the protection layer to suppress the leakage paths through the weak points in the SiO_2 layer. Then, Si NCs were deposited on the tunnel oxide at 600 °C for 15 s in a low-pressure chemical vapor deposition (LPCVD) furnace followed by Ge selective growth on top of Si NCs at 400 °C and 200 mTorr. After Ge/Si HNCs growth, in the same chamber, a Si cap layer was deposited to cover the Ge/Si HNCs. By controlling the deposition pressure and temperature, extra Si growth on oxide, where no Ge/Si HNCs are covered can be effectively suppressed. The typical growth temperature and pressure is around 500 °C and 50 mTorr, respectively. The fact that there is no extra Si growth was confirmed by the similar NC density before and after the cap layer deposition, because otherwise the density would become higher after the cap layer deposition. In addition, we used a reference SiO_2 sample, where no Ge/Si HNCs were pregrown to monitor the Si growth under the cap layer deposition conditions. No NC was found on that sample. The intention to deposit this Si cap layer is to protect the Ge from being oxidized in the following control oxide deposition step. In this step, SiH_4 and O_2 flow onto the sample at 400 °C at which Ge would be easily oxidized without cap layer protection. Essentially, our Ge/Si HNCs are Si shell/Ge core-like HNCs. Control oxide of about 25 nm was deposited at 400 °C followed by polysilicon gate deposition. Ohmic contacts were formed on source, drain, and gate to complete the device fabrication.

III. Results and Discussion

Fig. 1(a) shows the device cross section of Ge/Si HNC memory and Fig. 1(b) shows the schematic band diagram of Ge/Si HNC memory, where the band offsets were derived from bulk materials. Type-II band alignment provides a deeper quantum well formed at Ge side, which benefits long time hole storage in Ge. It should be pointed out that the Coulomb blockade and quantum confinement [20]–[24] do, to some level, affect the band offset between Ge and Si considering their nanoscale size, however, one cannot readily obtain an accurate bandstructure of this Ge/Si HNC system due to the fact that the shape of the HNCs is arbitrary and the degree of Ge/Si interdiffusion is unknown. Therefore, Fig. 1(b) is only tentative, and more accurate band alignment structure of this Ge/Si HNC system needs further investigations using 3-D atomistic level simulations.

Fig. 2(a) and (b) show the scanning electron microscopy (SEM) images of Si NCs and Ge/Si HNCs, respectively. The dot density of both Si NCs and Ge/Si HNCs is around 6×10^{11} cm^{-2}, while the average size of Ge/Si HNCs is slightly larger than that of Si NCs, which indicates the good self-

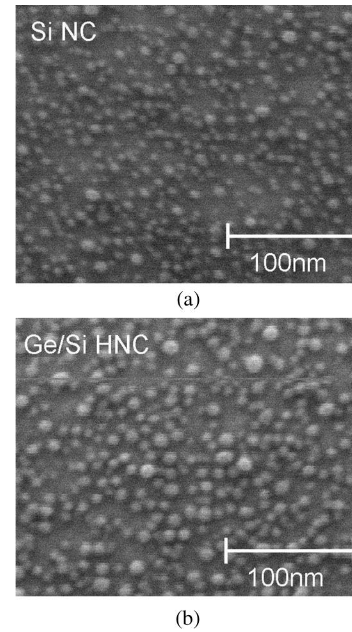

Fig. 2. SEM images of (a) Si NCs and (b) Ge/Si HNCs.

assembly of Ge on Si. The histograms of size distribution of Ge/Si HNCs and Si NCs are plotted and shown in Fig. 3(a) and (b). The mean size of Si NCs and Ge/Si HNCs are 5.96 and 6.96 nm, respectively. Since these numbers are obtained from SEM investigation, they represent more or less the "base" diameter of the NCs, suggesting the larger size of the HNCs. We can speculate that the "height" of these HNCs is also larger although the accurate value was not determined due to the limitation of SEM imaging and tip effect of an atomic force microscope (AFM) [14]. The self-aligned growth of Ge on Si dots was also confirmed by X-ray photoelectron spectroscopy (XPS) measurements and AFM results [14]. It should be noted that similar selective growth of Ge on Si has been investigated intensively [25]–[31], which have shown that Ge can be grown on patterned islands of Si to obtain a controllable arrangement of Ge/Si heteroisland. For example, Ichikawa's group reported their results [31] on selective epitaxial growth of Ge nanoislands and Si/Ge nanoislands on Si windows by introducing GeH_4 and Si_2H_6 gas.

MOS capacitors with Ge/Si HNCs and Si NCs embedded in the SiO_2 were characterized by capacitance–voltage (*C*–*V*) sweep measurements. The measurement was carried out by sweeping from the inversion to accumulation, and then, back to inversion again. Fig. 4(a) shows the high frequency (1 MHz), ±15 V *C*–*V* sweeps of Ge/Si HNC and Si NC memories. With the same device size and sweep range, larger memory window is observed in Ge/Si HNC capacitor compared to Si only NC capacitor, which indicates that Ge/Si HNC memory has a larger storage capacity. Fig. 4(b) shows the dependence of memory window on the sweep voltages of Ge/Si HNCs memory, further confirming the memory effect of our devices because the memory window increases with the scanning gate voltage. No such hysteresis is found in control device, where no NCs were embedded between control oxide and tunnel oxide, as shown

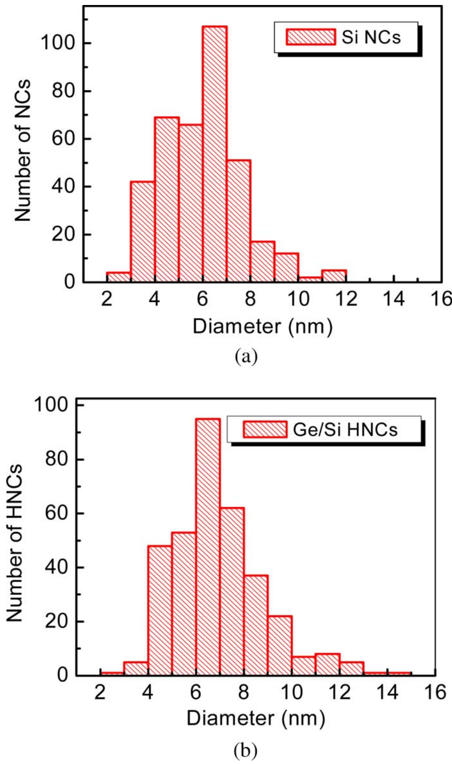

Fig. 3. Histograms of (a) Si NCs and (b) Ge/Si HNCs size distribution.

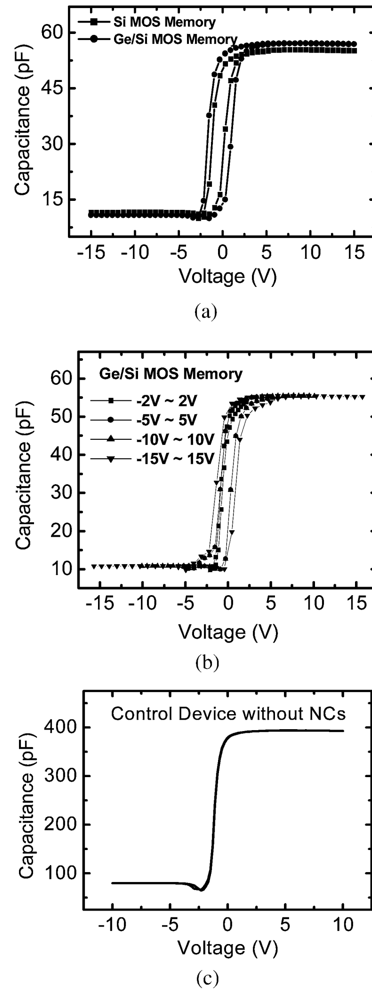

Fig. 4. (a) Ge/Si HNC and Si NC MOS memories *C–V* sweep under the same sweep range. (b) *C–V* sweep of Ge/Si HNC MOS memory under different sweep range. (c) *C–V* sweep of control device with no NCs.

in Fig. 4(c). This means that the oxide quality is good and the memory effect shown in the Ge/Si HNC and Si NC memories is due to the charge stored in the NCs rather than the defect or interface states charging.

Fig. 5 shows the retention characteristics of Ge/Si HNC and Si NC MOS memories. After programming of holes onto the floating gate with gate bias of –20 V for 2 s, the transient capacitance (C_t) was recorded every 30 ms. Flat band voltage ($V_{\rm FB}$) shift is deduced by subtracting the voltage at C_t on the fresh *C–V* curve from the initial $V_{\rm FB}$, where the capacitance starts to be recorded. It is shown that after 10^4 s, the percentage of hole charge loss of Ge/Si HNC memory is only half compared with Si NC memory, which confirms that an additional quantum well exists in Ge side of the HNCs. The charge decay for Ge/Si HNC and Si NC memories is a bit fast due to the stress (read voltage) applied on the gate when C_t was simultaneously being recorded. Nevertheless, relatively slower charge leakage in HNC capacitor device suggests that longer retention is achieved by introducing Ge on Si as the floating gate, which is affirmed in the MOSFET memory performance comparison later.

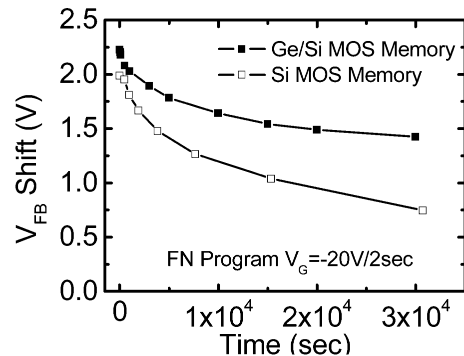

Fig. 5. Hole charge retention characteristics of Ge/Si HNC and Si NC MOS memories.

Fig. 6 shows three I_D-V_G curves, from left to right, corresponding to programmed, neutral, and erased states of the Ge/Si HNC MOSFET memory, respectively. The gate bias conditions for programming and erasing are -15 V/4 s and $+16$ V/4 s, respectively. The shift of $I_D - V_G$ curves indicates an evident memory effect. The threshold voltage value (V_T) represents the amount of the electrons/holes charged on the NCs. As shown in Fig. 6, V_T increases (absolute value) in programming and decreases in erasing. It is found that V_T at erased state is smaller than neutral state. It is understandable considering that electron injection dominates the erasing process. After neutralizing the charged holes during programming, extra electrons were injected and stored in the NCs to shift the V_T to smaller value than neutral state. The reason that electron injection dominates the erasing process is because of the smaller effective mass

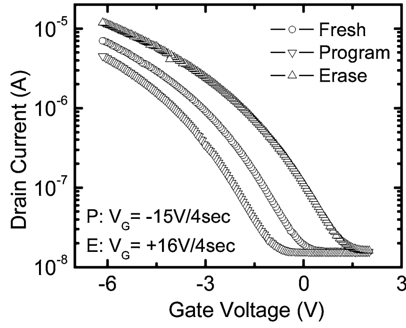

Fig. 6. Transfer characteristics of Ge/Si HNC MOSFET memory under fresh, FN programmed, and FN erased conditions.

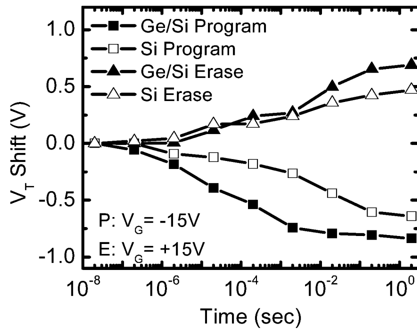

Fig. 7. Hole charge programming and erasing characteristics of Ge/Si HNC and Si NC MOSFET memories.

of electron and the lower injection energy barrier for electron, compared to hole.

Fig. 7 shows programming and erasing characteristics of the Ge/Si HNC and Si NC memory devices. Gate bias of -15 and $+15$ V were used to program and erase the devices. After 2 s, both programming and erasing get saturated because of the Coulomb blockade effect in nanoscale materials. Faster programming and a comparable erasing speed are observed in Ge/Si HNC memory compared with Si NC memory. Faster programming speed of Ge/Si HNCs relates to the fact that deeper quantum well in Ge/Si HNC creates more energy levels compared to Si NC and the similar erasing speed is understandable considering that the electrons tunneling from channel to NCs dominates the whole erasing process. Larger memory window in Ge/Si HNC memory (the voltage difference between the erased and programmed states) is due to more energy levels in larger Ge/Si well than Si well.

Fig. 8 is the retention performance comparison between Ge/Si HNC and Si NC memories, which plots threshold voltage shift as a function of waiting time. Programming condition is gate bias of -15 V for 4 s to fully charge the device before the threshold voltage is recorded. There was no stress applied in-between measurement points, which explains why the retention time for MOSFET memory appears much longer than that from the MOS capacitor memories, where flat band voltage was recorded with gate bias applied. Slower hole charge decay was found in Ge/Si HNC memory, especially at the early retention stage. This is because, for Ge/Si HNC memory, most of the holes prefer to store inside the Ge NCs. To leak back to the channel, these

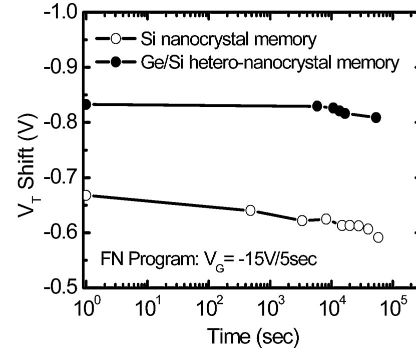

Fig. 8. Hole charge retention characteristics of MOSFET memory with Ge/Si HNCs and Si NCs as floating gate after FN programming.

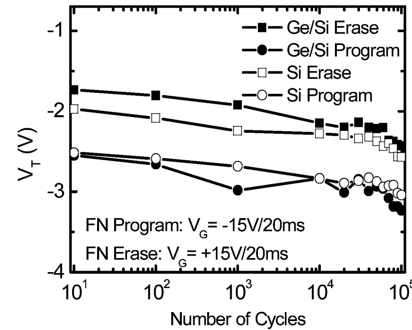

Fig. 9. Endurance characteristics of Ge/Si HNC and Si NC MOSFET memories. Programming and erasing are through FN operations.

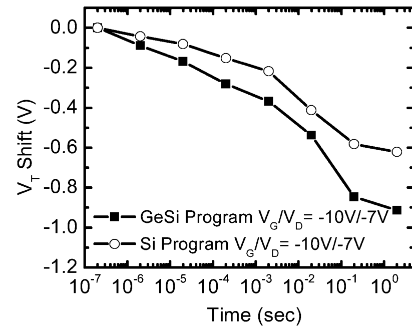

Fig. 10. Hole HCI programming characteristics of Ge/Si HNC and Si NC memories.

holes have to be thermally activated to overcome the Si NC barrier first, before it can tunnel through the tunnel oxide and back to the channel. While for Si NC memory, charging of the defect levels within Si NCs dominates the programming process. Defect-related charging is not reliable [32].

Fig. 9 shows the endurance characteristics of Ge/Si HNC and Si NC memories. The programming and erasing conditions are -15 V/20 ms and $+15$ V/20 ms, respectively. Both devices exhibit good endurance behavior up to 10^5 cycles of operation.

In addition to FN operation, HCI programming was also used to operate the devices and the device performance was compared between Ge/Si HNC and Si NC memories. Fig. 10 shows HCI programming characteristics of Ge/Si HNC and Si NC memories. Both gate voltage and drain voltage affect the programming speed. A large threshold voltage shift of about

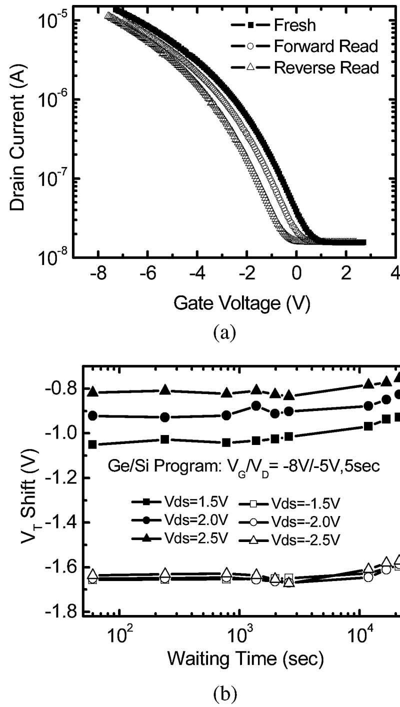

Fig. 11. (a) $I_D - V_G$ curves at fresh and HCI programmed modes, including reverse and forward read conditions. (b) Threshold voltage shift measured in forward and reverse read conditions after HCI programming of the Ge/Si HNC memory.

0.913 V can be achieved under $V_G = -10$ V and $V_D = -7$ V for 2 s in the Ge/Si HNC memory. As shown in Fig. 10, similar to FN programming characteristics, Ge/Si HNC memory exhibits faster programming speed with HCI programming.

After hot carrier programming, most charges have been written into the HNCs near the drain side while those NCs near the source side are partially charged or uncharged. Therefore, two threshold voltage states can be obtained when the device is read from drain side (forward read) and source side (reverse read), respectively. Fig. 11(a) shows $I_D - V_G$ curves at fresh, reverse, and forward read conditions, indicating different threshold voltage shift. Fig. 11(b) shows threshold voltage shift measured in forward and reverse read conditions after HCI programming of the Ge/Si HNC memory. Two sets of threshold voltage shift are clearly observed. Different threshold voltage shift with different drain voltage during forward reading is because the bias on drain side effectively changes the barrier height for the channel carriers, while during reverse read, this barrier height is insignificantly affected by small read voltages, which explains independence of threshold voltage shift on the source side bias.

While p-channel MOSFET Ge/Si HNC memory exhibits superior hole storage because of the type-II energy band alignment between Ge and Si, it is interesting to investigate electron storage due to its small effective mass and less damage during the operation. Other than deeper potential well between valance band of Ge and Si for holes storage, there also exists a potential well between conduction band of Si NC and SiO_2 for electrons storage as shown in Fig. 1(b). Basically band-to-band tunneling was used for hot electron injection. Fig. 12 shows how this injection

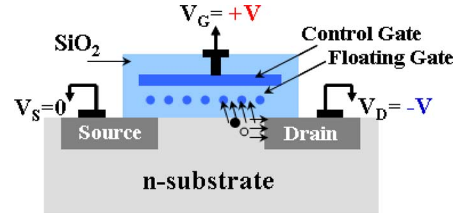

Fig. 12. Schematic of hot electron injection operation.

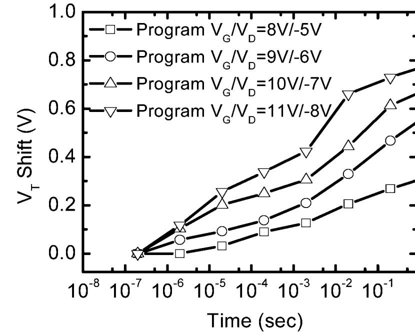

Fig. 13. Electron charge HCI programming characteristics of Ge/Si HNC memory with four sets of control gate and drain bias.

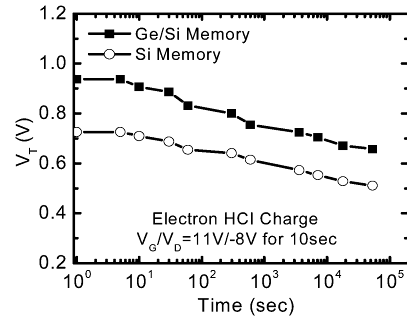

Fig. 14. Electron charge HCI programming and FN erasing characteristics of Ge/Si HNC and Si NC memories.

occurs. A positive gate voltage and negative drain voltage are applied so that p^+-drain/n-channel junction is reverse-biased. The electrons generated in this junction via band-to-band tunneling can be redirected into the floating dots near the drain side under the electrical field between gate and channel. Therefore, the threshold voltage sensed from drain and source side is different because of this locally charged floating gate. Similar programming scheme for using electron to program p-channel device was reported by other researchers [33].

Fig. 13 shows the transient electron charging characteristics of Ge/Si HNC memory using HCI to program. The efficiency of the programming is improved with increasing bias combination of control gate and drain, and this phenomenon was also found in holes storage characteristics. Fig. 14 shows the programming and erasing characteristics of Ge/Si HNC and Si NC memories using HCI to program and FN to erase the electrons. With HCI programming, memory windows of 0.813 and 0.668 V are reached in Ge/Si HNC and Si NC memories, respectively, with control gate and drain bias of 10 V/−7 V for 2 s. The slightly larger memory window in Ge/Si HNC memory indicates that

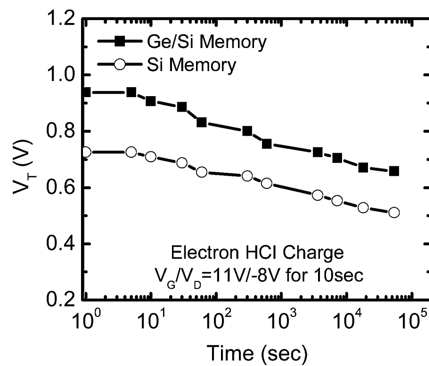

Fig. 15. Electron charge retention of Ge/Si HNC and Si NC memories after HCI programming. The programming condition is indicated in the figure.

during programming not only Si NC is charged, but also Ge NC and interface level charging play a role to the threshold voltage shift. The programming and erasing speeds do not show much difference between Ge/Si HNC and Si NC memories and it is due to the fact that electrons are charged/discharged through the Si NCs in both devices. Fig. 15 shows the electron retention characteristics of Ge/Si HNC and Si NC memories. The devices were programmed with gate and drain bias of 11 and -8 V, respectively, for 10 s. The charge decay within the 15 h for Ge/Si HNC and Si NC memories are very similar. The electron retention is worse than hole retention as shown in Fig. 10(b) due to the shallower electron barrier in the conduction band edge.

IV. Conclusion

Ge/Si self-assembled HNCs with high density were grown using LPCVD. MOS capacitors and MOSFET memory devices with Ge/Si HNCs and Si NCs embedded between control and tunnel oxide were fabricated with the same process flow. Both FN and HCI programming were used to operate the devices. Enhanced performance of Ge/Si HNC memory is achieved compared to Si NC memory, including improved retention time, faster programming speed, and larger charge storage capability.

References

[1] S. Tiwari, F. Rana, K. Chan, H. Hanafi, W. Chan, and D. Buchanan, "Volatile and nonvolatile memories in silicon with nano-crystal storage," in *Proc. IEDM Tech. Dig.*, 1995, pp. 521–524.

[2] S. Tiwari, R. Rana, K. Chan, L. Shi, and H. Hanafi, "Single charge and confinement effects in nano-crystal memories," *Appl. Phys. Lett.*, vol. 69, pp. 1232–1234, Aug. 1996.

[3] R. Muralidhar, R. F. Steimle, M. Sadd, R. Rao, C. T. Swift, E. J. Prinz, J. Yater, L. Grieve, K. Harber, B. Hradsky, S. Straub, B. Acred, W. Paulson, W. Chen, L. Parker, S. G. H. Anderson, M. Rossow, T. Merchant, M. Paransky, T. Huynh, D. Hadad, K. M. Chang, and B. E. White, Jr., "A 6 V embedded 90 nm silicon nanocrystal nonvolatile memory," in *Proc. IEDM Tech. Dig.*, 2003, pp. 26.2.1–26.2.4.

[4] G. Puzzilli and F. Irrera, "Data retention of silicon nanocrystal storage nodes programmed with short voltage pulses," *IEEE Trans. Electron Devices*, vol. 53, no. 4, pp. 775–781, Apr. 2006.

[5] C. Y. Ng, T. P. Chen, M. Yang, J. B. Yang, L. Ding, C. M. Li, A. Du, and A. Trigg, "Impact of programming mechanisms on the performance and reliability of nonvolatile memory devices based on Si nanocrystals," *IEEE Trans. Electron Devices*, vol. 53, no. 4, pp. 663–667, Apr. 2006.

[6] Y. C. King, T. J. King, and C. Hu, "MOS memory using germanium nanocrystals formed by thermal oxidation of $Si_{1-x}Ge_x$," in *Proc. IEDM Tech. Dig.*, 1998, pp. 115–118.

[7] M. She and T. J. King, "Impact of crystal size and tunnel dielectric on semiconductor nanocrystal memory performance," *IEEE Trans. Electron Devices*, vol. 50, no. 9, pp. 1934–1940, Sep. 2003.

[8] B. H. Koh, E. W. H. Kan, W. K. Chim, W. K. Choi, D. A. Antoniadis, and E. A. Fitzgerald, "Traps in germanium nanocrystal memory and effect on charge retention: Modeling and experimental measurements," *J. Appl. Phys.*, vol. 97, pp. 124305-1–124305-9, Jun. 2005.

[9] D. T. Zhao, Y. Zhu, R. G. Li, and J. L. Liu, "Cobalt silicide nanocrystal memory," in *Proc. Device Res. Conf. Dig.*, 2005, pp. 105–106.

[10] P. H. Yeh, C. H. Yu, L. J. Chen, H. H. Wu, and P. T. Liu, "Low-power memory device with $NiSi_2$ nanocrystals embedded in silicon dioxide layer," *Appl. Phys. Lett.*, vol. 87, pp. 193504-1–193504-3, Nov. 2005.

[11] P. K. Singh, K. K. Singh, R. Hofmann, K. Argstrong, N. Krishna, and S. Mahapatra, "Au nanocrystal memory reliability and failure analysis," in *Proc. IPFA 2008*, Jul., pp. 1–5.

[12] F. M. Yang and T. C. Chang, "Memory characteristics of Co nanocrystal memory device with HfO_2 as blocking oxide," *Appl. Phys. Lett.*, vol. 90, pp. 132102-1–132102-3, Mar. 2007.

[13] J. J. Lee, X. Wang, W. Bai, N. Lu, J. Liu, and D. L. Kwong, "Theoretical and experimental investigation of Si NC memory device with HfO_2 high-κ tunneling dielectric," in *Proc. VLSI Symp. Tech. Dig.*, 2003, pp. 33–34.

[14] B. Li, J. L. Liu, G. F. Liu, and J. A. Yarmoff, "Ge/Si heteronanocrystal floating gate memory," *Appl. Phys. Lett.*, vol. 91, pp. 132107-1–132107-3, Sep. 2007.

[15] H. G. Yang, Y. Shi, L. Pu, R. Zhang, B. Shen, P. Han, S. L. Gu, and Y. D. Zheng, "Nonvolatile memory based on Ge/Si hetero-nanocrystals," *Appl. Surf. Sci.*, vol. 224, no. 1–4, pp. 394–398, Mar. 2004.

[16] D. T. Zhao, Y. Zhu, R. G. Li, and J. L. Liu, "Simulation of a Ge-Si hetero-nanocrystal memory," *IEEE Trans. Nanotechnol.*, vol. 5, no. 1, pp. 37–41, Jan. 2006.

[17] Y. Zhu, D. T. Zhao, and J. L. Liu, "Numerical investigation of transient capacitances of Ge/Si heteronanocrystal memories in retention mode," *J. Appl. Phys.*, vol. 101, pp. 034508-1–034508-4, Feb. 2007.

[18] F. M. Yang, T. C. Chang, P. T. Liu, P. H. Yeh, U. S. Chen, Y. C. Yu, J. Y. Liu, S. M. Sze, and J. C. Lou, "Using double layer $CoSi_2$ nanocrystals to improve the memory effects of nonvolatile memory devices," *Appl. Phys. Lett.*, vol. 90, pp. 212108-1–212108-3, May 2007.

[19] Y. Zhu, B. Li, J. L. Liu, G. F. Liu, and Y. A. Yarmoff, "$TiSi_2$/Si heteronanocrystal metal-oxide-semiconductor-field-effect-transistor memory," *Appl. Phys. Lett.*, vol. 89, pp. 233113-1–233113-3, Dec. 2006.

[20] W. Guan, S. Long, M. Liu, Q. Liu, Y. Hu, Z. Li, and R. Jia, "Modeling of retention characteristics for metal and semiconductor nanocrystal memories," *Solid-State Electron.*, vol. 51, pp. 806–811, May 2007.

[21] M. She and T. J. King, "Impact of crystal size and tunnel dielectric on semiconductor nanocrystal memory performance," *IEEE Trans. Electron Devices*, vol. 50, no. 9, pp. 1934–1940, Sep. 2003.

[22] Y. M. Niquet, G. Allan, C. Delerue, and M. Lannoo, "Quantum confinement in germanium nanocrystals," *Appl. Phys. Lett.*, vol. 77, pp. 1182–1184, Aug. 2000.

[23] T. van Buuren, L. N. Dinh, L. L. Chase, W. J. Siekhaus, and L. J. Terminello, "Changes in the electronic properties of Si nanocrystals as a function of particle size," *Phys. Rev. Lett.*, vol. 80, no. 17, pp. 3803–3806, Apr. 1998.

[24] C. Bostedt, T. van Buuren, T. M. Willey, N. Franco, L. J. Terminello, C. Heske, and T. Moller, "Strong quantum-confinement effects in the conduction band of germanium nanocrystals," *Appl. Phys. Lett.*, vol. 84, no. 20, pp. 4056–4058, May 2004.

[25] J.-H. Zhu, K. Brunner, and G. Abstreiter, "Two-dimensional ordering of self-assembled Ge islands on vicinal Si(001) surfaces with regular ripples," *Appl. Phys. Lett.*, vol. 73, no. 5, pp. 620–622, Aug. 1998.

[26] T. Kamins and R. Williams, "Lithographic positioning of self-assembled Ge islands on Si(001)," *Appl. Phys. Lett.*, vol. 71, no. 9, pp. 1201–1203, Sep. 1997.

[27] Q. Li, S. M. Han, S. R. J. Brueck, S. Hersee, Y. B. Jiang, and H. Xu, "Selective growth of Ge on Si (100) through vias of SiO_2 nanotemplate using solid source molecular beam epitaxy," *Appl. Phys. Lett.*, vol. 83, no. 24, pp. 5032–5034, Dec. 2003.

[28] K. Sumitomo, F. Lin, Y. Homma, and T. Ogino, "Selective formation of Ge nanostructures on Si (111) surface with patterned steps," *Appl. Surf. Sci.*, vol. 237, no. 1–4, pp. 68–74, Oct. 2004.

[29] T. S. Yoon, Z. Zhao, J. Liu, Y. H. Xie, D. Y. Ryu, T. P. Russell, H. M. Kim, and K. B. Kim, "Selective growth of Ge islands on nanometer-scale patterned SiO_2/Si substrate by molecular beam epitaxy," *Appl. Phys. Lett.*, vol. 89, pp. 063107-1–063107-7, Aug. 2006.

[30] E. S. Kim, N. Usami, and Y. Shiraki, "Control of Ge dots in dimension and position by selective epitaxial growth and their optical properties," *Appl. Phys. Lett.*, vol. 72, no. 13, pp. 1617–1619, Mar. 1998.
[31] Y. Nitta, M. Shibata, K. Fujita, and M. Ichikawa, "The nanometer-scale selective overgrowth of Ge over Si islands on Si (001) windows in ultrathin SiO_2 films," *Surface Sci.*, vol. 496, no. 1–2, pp. L7–L12, Jan. 2002.
[32] Y. Shi, K. Saito, H. Ishikuro, and T. Hiramoto, "Characteristics of narrow channel MOSFET memory based on silicon nanocrystals," *Jpn. J. Appl. Phys.*, vol. 38, no. 4B, pp. 2453–2456, Apr. 1999.
[33] J. T. Park, J. Y. Chun, H. K. Kim, S. J. Jang, and C. G. Yu, "New programming and erasing schemes for p-channel flash memory," *IEEE Electron Device Lett.*, vol. 21, no. 10, pp. 491–493, Oct. 2000.

Bei Li received the B.Sc. and M.S. degrees in materials science and engineering from Zhejiang University, Zhejiang, China, in 2000 and 2003, respectively. She is currently working toward the Ph.D. degree in electrical engineering with the University of California, Riverside, CA.

Her current research interests include nanoscale materials synthesis for nonvolatile memory application.

Jianlin Liu (S'99–M'02) received the B.S. and Ph.D. degrees in physics from Nanjing University, Nanjing, China, in 1993 and 1997, respectively, and the Ph.D. degree in electrical engineering from the University of California, Los Angeles, CA, in 2003.

In March 2003, he joined as a member of Tenure-track Faculty with the Department of Electrical Engineering, University of California, Riverside, CA, where he is currently an Associate Professor. He is the author or coauthor of more than 160 technical journal papers and conference proceedings, and three book chapters. His current research interests include Group-IV and ZnO-based semiconductor and diluted magnetic semiconductor thin films, nanowires, and quantum dots, and their nanoelectronic and optoelectronic devices.