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Realization of silicon quantum wires by selective chemical etching and thermal oxidation

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Abstract Ultra-fine silicon quantum wires with SiO_2 boundaries were successfully fabricated by combining SiGe/Si heteroepitaxy, selective chemical etching and subsequent thermal oxidation. The results are observed by scanning electron microscopy. The present method provides a very controllable way to fabricate ultra-fine silicon quantum wires, which is fully compatible with silicon microelectronic technology. As one of the key processes of controlling the lateral dimensions of silicon quantum wires, the wet oxidation of silicon wires has been investigated, self-limiting wet oxidation phenomenon in silicon wires is observed. The characteristic of the oxidation retardation of silicon wires is discussed.

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Artificially modulated silicon-based structures with reduced dimensions such as silicon quantum wires (SQWRs) have recently attracted great interest for both potential device applications and novel physical phenomena. In order to study this field thoroughly, the first step is to establish valuable fabrication methods of ultra fine SQWRs. Up to now, most of the quantum wires have been made by fabricating a grating-like gate on top of a two-dimensional electron gas contained in a semiconductor heterojunction or metal-oxide semiconductor structures [1–3]. By applying a negative gate voltage, the system can be turned from the two- to the one-dimensional regime, where electron confinement is achieved by the electrostatic confining potential. However, only few methods have been developed to obtain ultra-fine SQWRs and establish one-dimensional confinement by physical boundaries [4–7]. A thermal oxidation method was used to thin silicon columns to form silicon nanostructures [4], which may present a method of fabricating SQWRs fully contained within the SiO_2 acting as high potential barrier: The fabrications of the array of SQWRs with SiO_2/Si interfaces laying on silicon substrate by anisotropic wet chemical etching and thermal oxidation were reported [5, 6]; A silicon single electron transistor operating at room temperature was studied by controlling the structure of a wire-patterned very thin silicon layer through pattern-dependent oxidation [7]. At the present stage, there still exists an urgent need for the development of fabrication techniques for obtaining high-quality SQWRs.

SiGe/Si heteroepitaxial film has many potential applications in silicon technology. It would be very useful to apply this film to the fabrication of various SQWRs and related devices due to its excellent properties such as high-quality epitaxial growth, selective etching and thermal oxidation. Formation of GeSi quantum wire arrays on a v-groove patterned silicon substrate by gas-source silicon molecular beam epitaxy was reported [8], and SiGe/Si multiple quantum well wires were successfully fabricated by using a selective chemical etching technique [9]. Recently, we presented a novel approach to fabricate ultra-fine SQWRs with the physical boundaries of SiO_2 based on a SiGe/Si heterostructure combining SiGe/Si heteroepitaxy, selective chemical wet etching and subsequent thermal oxidation [10]. Fig. 1 shows the fabrication steps of the SQWRs. First, a heteroepitaxial technique is utilized to grow a high-quality Si/SiGe/Si heteroepitaxial film on silicon substrate. On the trench structures generated by lithography and reactive ion etching, the selective chemical wet etching is applied to remove SiGe alloy layers and form silicon wires. Finally, thermal oxidation is carried out to obtain the expected SQWRs with SiO_2 boundaries. Furthermore, it has been shown that thermal oxidation of silicon wires is one of the key processes in fabricating ultra-fine SQWRs. It not only forms high quality Si/SiO_2 interfaces, but also smooths and reduces the lateral dimensions of the SQWRs. In this paper, the fabrication characteristics of SQWRs will be considered in detail. More discussions of the thermal oxidation of silicon wires will be given.

1 Experimental procedure

In this work, (100)-oriented p-type silicon wafers with a resistivity of $25 \sim 50\ \Omega$ cm were used as substrates. First,

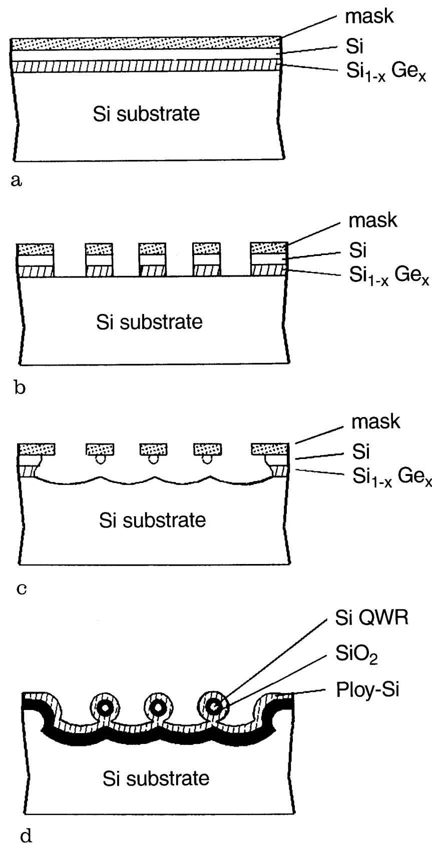

Fig. 1a–c. Fabrication steps of SQWRs. **a** Si/SiGe heteroepitaxy, **b** mask pattern and shallow trench formation, **c** selective chemical etching, and **d** thermal oxidation

the substrates were cleaned chemically by a modified Shiraki procedure [11]. A SiGe/Si heterostructure film was grown by very low pressure chemical vapor deposition (VLP-CVD) using SiH_4 and GeH_4 as source gas. The details of the growth technique have already been reported elsewhere [12]. A 100 nm thick silicon buffer layer was grown on the silicon substrate prior to the growth of the SiGe layer. The $Si_{0.8}Ge_{0.2}$ layer was grown between the buffer layer and superficial silicon layer (Fig. 1a). Using this epitaxial growth technique, the expected thickness of the superficial silicon layer can be easily achieved. Subsequently, mask and lithography techniques were carried out to generate line-and-space patterns on the Si/SiGe/Si heteroepitaxial film. Then, trenches were formed by reactive ion etching using SF_6 gas (Fig. 1b). Next, the selective chemical etchant consisting of HNO_3 : CH_3COOH: diluted HF solution at 25 °C was used to etch the trench structures to remove the $Si_{0.8}Ge_{0.2}$ layers and narrow the silicon wires (Fig. 1c). After clearing the mask off, the as-etched silicon wires were thermally oxidized in wet oxygen atmosphere in order to smooth the surface of the silicon wires and reduce the lateral dimensions to form expected ultra-fine SQWRs. Finally, the thermal oxidation in dry oxygen was carried out to obtain high-quality Si/SiO_2 interfaces (Fig. 1d).

For investigating the fabrication progression of SQWRs, the cross-sections of the fabricated SQWRs were observed by a scanning electron microscope (SEM). In order to clearly distinguish the SQWRs, a sample was deposited on a polysilicon film mask on SQWRs by the VLP-CVD reactor, and then was back-side polished and cleaved. The cleaved faces were delineative etched with a diluted HF for several minutes. This facilitated differentiation of the SQWRs and oxide. The space vacated by the oxide now appeared as a dark strip sandwiched between two bright areas of silicon and polysilicon. A thin layer of gold was then sputter-deposited on the exposed faces to alleviate sample charging. These procedures provided excellent contrast in the SEM image.

2 Results and discussions

2.1 Si/SiGe/Si heteroepitaxy

From Fig. 1, it has been noted that the whole fabrication process is based on a Si/SiGe/Si heterostructure and the final SQWRs come from the superficial silicon layer. Therefore, the realization of high-quality Si/SiGe/Si heteroepitaxial films with abrupt interfaces is a prerequisite for fabricating ultra-fine SQWRs. Fig. 2 shows the temperature dependence of the growth rates of silicon and SiGe alloy on Si (100) substrate in the VLP-CVD reactor with SiH_4 flow rate of 1.4 sccm. In the present work, the growth temperature is at 600 °C, and the growth rate is at the level of 1 Å/sec, which offers the capability of controlling atomically precise thicknesses and abrupt interfaces [12]. As an advantage of this type of process, the expected thickness of the superficial silicon layer can be easily achieved, which is important for controlling the lateral dimensions of the SQWRs. In general, decreasing the mole fraction of Ge in SiGe alloy is beneficial to obtaining high-quality heteroepitaxial films, whereas it is not good for having the high selectivity of the chemical etching. Hence, the optimum mole fraction of Ge is selected as 0.2. Here, the thickness of $Si_{0.8}Ge_{0.2}$ layer is below the critical thickness for introduction of misfit dislocations, the $Si_{0.8}Ge_{0.2}$ layer is pseudomorphically strained.

2.2 Selective chemical etching

The selective chemical wet etching techniques for SiGe/Si heteroepitaxial films have been developed for several years. The characteristics of several selective chemical etchants were investigated, it was demonstrated that HNO_3 : CH_3COOH : diluted HF was very good in reducing SiGe nanostructures [13]. Furthermore, the advantages of this etchant for the present fabrication process are that it is compatible with the mask and lithography processes, and the optimum etch rate and selectivity are well obtained by altering the etchant composition. Here, because the linewidth of the mask pattern is wider than the thickness of the superficial silicon layer, the etch rate for silicon is controlled within a fixed ratio of the constituents of the etchant in order to form the silicon wire having a quasisquare cross section. Through the selective chemical etching, the $Si_{0.8}Ge_{0.2}$ layer is removed and the

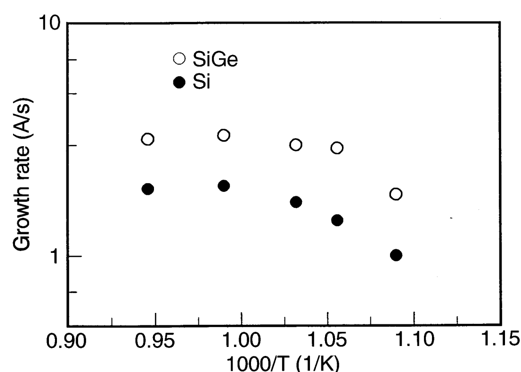

Fig. 2. Temperature dependence of the growth rates of Si and SiGe alloy on Si (100) substrate

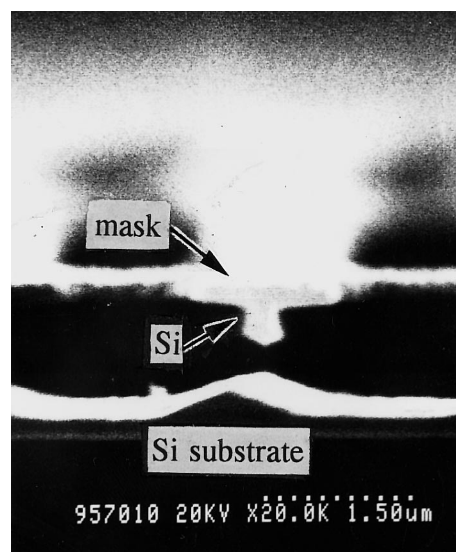

Fig. 3. Cross-sectional SEM image of an as-etched silicon wire

superficial silicon layer is narrowed to form silicon wires. Fig. 3 shows a cross-sectional SEM image of a silicon wire prepared by the selective chemical etching. The top layer above the silicon wire is the mask. Furthermore, a smooth and pit-free surface is demonstrated.

2.3 Thermal oxidation process

The advantages of dry thermal oxidation to fabricate controllable SQWRs have already been demonstrated [4–7]. Self-limiting oxidation phenomena related to oxide viscous stress in silicon nanostructures have been observed. It was seen as an opportunity for producing silicon nanostructures with $\pm$ 1 nm control in lateral dimensions in the self-limiting regime of oxidation temperatures below 950 °C [14]. For the present SiGe/Si nanostructure, though the SiGe layer below the silicon wires is completely etched away after the selective etching, it still remains at other parts of the sample. Hence, the thermal oxidation at high temperatures above 850 °C is forbidden because of the thermal stability of SiGe alloy, and the dry oxidation at low temperatures is not practical because of the length of time it takes to narrow silicon wires to expected lateral dimensions. Fortunately, the wet oxidation at low temperatures offers an important opportunity for realizing ultra-fine SQWRs. Therefore, two steps of wet and then dry oxidation are carried out, the latter one is used to obtain high quality Si/SiO_2 interfaces. Fig. 4 shows the cross-sectional SEM image of a SQWR embedded in the oxide after the thermal oxidation. Here, the radius of the SQWR is about 20 nm.

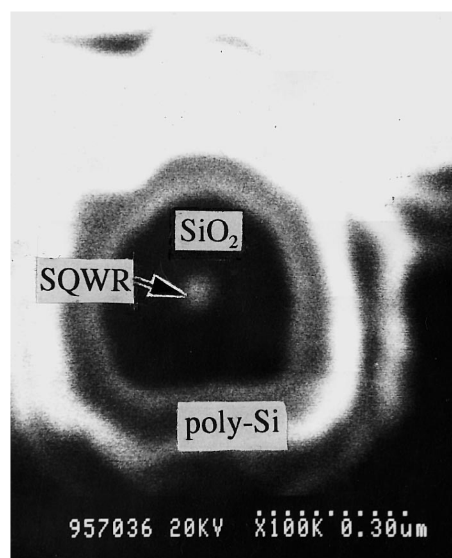

Fig. 4. Cross-sectional SEM image of a SQWR with the radius of ~ 20 nm

Obviously, understanding the wet-oxidation of silicon wires is important for fabricating well-controllable ultra fine SQWRs. It is desired that the self-limiting oxidation effect observed in dry oxidation could also occur in the present wet oxidation. For that reason, an investigation on the characteristics of wet oxidation at three temperatures of 850, 800 and 750 °C is performed. Fig. 5 shows the planar field oxide thickness on a flat surface and the silicon wire oxide thickness as a function of oxidation time for 850 °C wet oxidation. Prior to the thermal oxidation, a set of samples are prepared under the same etching conditions to minimize silicon wire variations among the samples. The typical starting diameter of an as-etched wire is about 250 nm. Dimensional data are obtained from the SEM micrographs. As oxidation progresses, the oxide thickness on the planar field continues to increase linearly with the time, while the oxidation rate of silicon wire appears to be decreasing with the increase in oxidation time. The wet oxidation results at the other two lower temperatures, 800 and 750 °C are found to exhibit similar behavior as that found at 850 °C. Further, the trend of the data shows that the oxide thicknesses appear to saturate to similar asymptotic values of 180 nm for these oxidation temperatures. As seen clearly in the following observations, the limiting value of 180 nm for 800 and 850 °C indicates that the silicon wires have been oxidized out

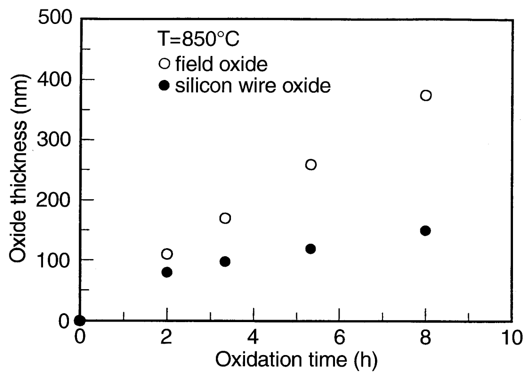

Fig. 5. Oxide thicknesses vs oxidation time for 850 °C wet oxidation

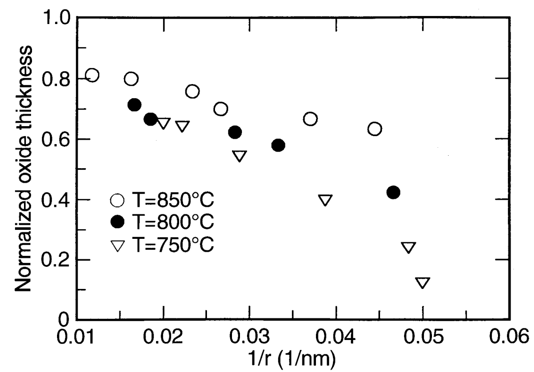

Fig. 7. Oxide thickness on SQWR surfaces normalized to that on the flat surface as a function of the inverse of the radius of the SQWRs for 850, 800 and 750 °C wet oxidation, respectively

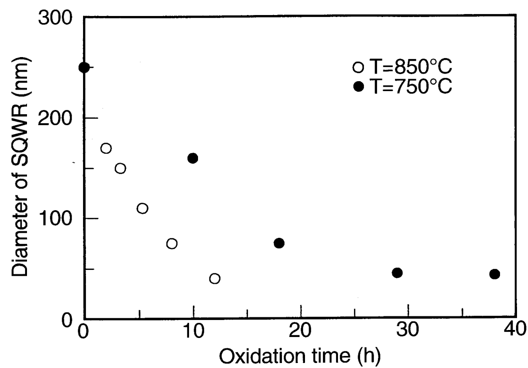

Fig. 6. Radii of SQWRs as a function of the oxidation time for 850, and 750 °C wet oxidation, respectively

while that for 750 °C demonstrates that the self-limiting oxidation phenomenon occurs under this oxidation temperature. Fig. 6 shows the radii of silicon wires reduce with the oxidation time at 850 and 750 °C, respectively. As the wet oxidation progresses, oxidation retardation of silicon wires is observed at these temperatures. As shown in Fig. 6, the retardation of oxidation becomes obvious with decreasing radius of the silicon wire and it also depends strongly on the oxidation temperature. It is found that the retardation of oxidation is more pronounced at 750 °C. After 20 hour of oxidation at 750 °C, the reduction rate of the diameter of the SQWR becomes extremely slow. The SQWRs have not disappeared even if the oxidation time gets to 38 hour. Moreover, the final diameter seems to self-limit to 40 nm here. The self-limiting oxidation phenomenon is not observed for wet oxidation at 850 °C. It is confirmed that the SQWRs vanish after 16 hour of oxidation. Fig. 7 clearly demonstrates the radius and temperature dependence of the retardation, where the vertical axis is the oxide thickness on silicon wire surfaces normalized to that on the flat surface, and the horizontal axis denotes the inverse of the radii of silicon wires after oxidation. The characteristic, as shown in Fig. 7, is similar to the observations reported previously [4, 15]. The oxidation retardation can usually be contributed to the additional stress from nonplanar viscous deformation of oxide [15]. Since the molecular volume of SiO_2 is more twice as large as the atomic volume of Si, consequently, the newly formed oxide expands and pushes out the old oxide. Owing to the very high viscosity of oxide, nonplanar two-dimensional viscous deformation of the oxide produces large additional stress. This viscous stress makes the oxidation reaction at the silicon surface more difficult. Based on the present observations, it is apparent that the extent of the oxidation retardation follows the change in the viscous stress with the oxidation temperature and the radius of silicon wires. The temperature dependence of the retardation is mainly associated with that of the oxide viscosity. The viscosity becomes higher at lower temperatures and, the stress increases at lower temperatures, consequently, leading to more retardation. In addition, it has to be noted that the self-limiting oxidation phenomenon in the present wet oxidation is found to occur at the temperature of 750 °C, which is about 200 °C lower than that observed in dry oxidation [4]. This may be due to the viscous stress of wet oxide being lower than that of dry oxide. The more severe retardation for smaller radii is the result of higher stress produced by more drastic deformation of the oxide. For the silicon wires with smaller radii, the old oxide layer has to expand more to accommodate a given increase in volume for each subsequent reaction. This causes a greater stress normal to the interface, retarding the process of further oxidation. There are two likely mechanisms for explaining the influence of the viscous stress on the oxidation retardation. One is that the surface reaction coefficient *Ks* is reduced by the normal viscous stress at the Si-SiO_2 interface [15]. Another is that oxidation diffusion is limited in a highly stressed oxide [14]. Up to now, there are still insufficient data to construct a unique predicative model for explaining all the oxidation phenomena associated with silicon nanostructures. Further studies are needed to identify the effects of the viscous stress on oxidation kinetic parameters. From the limited number of experiments at this time several interesting wet oxidation phenomena have already been observed. Oxidation retardation of silicon wires was observed to be greatly magnified and exhibits a self-limiting effect for wet oxidation at temperatures about 750 °C, which is very beneficial for fabricating controllable ultra fine SQWRs.

3 Conclusions

We have successfully fabricated ultra-fine SQWRs having Si/SiO_2 interfaces as physical boundary. This is accomplished by first growing a high quality Si/SiGe/Si heteroepitaxial film on silicon substrate by VLP-CVD, followed by lithography and reactive ion etching to form trench structures. Subsequently, the selective chemical wet etching with the solution of $HNO_3:CH_3COOH$: diluted HF at 25 °C is applied to remove $Si_{0.8}Ge_{0.2}$ alloy layer and form silicon wires. Finally, two steps of wet- and then dry-thermal oxidation are carried out to obtain ultra-fine SQWRs having Si/SiO_2 interfaces. Excellent results observed are evidenced by SEM. Furthermore, the characteristics of wet oxidation of silicon wires have been investigated. A self-limiting wet oxidation effect in silicon wires is observed, which is important for controlling the lateral dimensions of SQWRs. The present work has clearly shown the success of combining SiGe/Si heteroepitaxy, selective chemical wet etching and subsequent thermal oxidation as a very valuable method for fabricating ultra-fine SQWRs.

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