Synthesis of high-density PtSi nanocrystals for memory application

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Vapor-solid-solid growth mechanism was employed to synthesize PtSi nanocrystals with density of 1.5×10^{12} cm^{-2} by introducing SiH_4 onto Pt-catalyzed SiO_2/Si substrate. The nanocrystal density and average size were measured by scanning electron microscope and the nanocrystal chemical nature was determined by x-ray photoelectron spectroscope. Metal-oxide-semiconductor memory with PtSi nanocrystals was fabricated and characterized, showing very good memory performance. © *2010 American Institute of Physics*. [doi:10.1063/1.3421546]

Nonvolatile memory with discrete-trap type storage nodes attracts much attention as a promising candidate for future low power electronics. Si nanocrystal (NC) memory, introduced by Tiwari,[1] has been investigated tremendously at both academia and industry due to its potential to exceed the performance limits of conventional flash memories. Although superior performance was demonstrated in Si NC memory, the device reliability remains an issue because of the defect-related charge storage in Si NCs. It is difficult to control the trap levels and densities to achieve a consistency in retention because trap formation and annihilation are sensitive to high-temperature processes such as source/drain dopant activation annealing. To solve this problem, many other NCs,[2–5] and engineered gate structures[6,7] were proposed.

In this paper, we report the fabrication and characterization of high-density PtSi NC metal-oxide-semiconductor (MOS) memories. PtSi NCs were formed by vapor-solid-solid (VSS) growth mechanism, where Si precursor was introduced into Pt thin film-covered SiO_2/Si substrate at a subeutectic temperature. Traditionally, VSS was only used for nanowire (NW) research,[8] however the initial stage of the VSS growth to form silicide dots before the formation of NWs can be interesting for NC memory applications. Figure 1 shows energy band diagram of the memory device with PtSi NCs as floating gate. The work function of bulk PtSi, 4.9 eV,[9] is used to draw the diagram. Therefore, the Fermi level of PtSi is within the band gap of Si and the conduction band offset between PtSi and SiO_2 is 3.95 eV, 0.85 eV higher than that of Si NC memory, leading to longer retention time for electron storage. Other advantages of using PtSi NCs as floating gate for memory include easy and simple fabrication procedure, good thermal stability, high storage capability, and fast operation. These merits play important roles in future scaled memory technologies.

The device fabrication starts with a p-Si (100) substrate. Prediffusion cleaning was carried out and a thin thermal oxide of 3 nm was grown on the substrate at 850 °C. A very thin layer of metal catalyst film was deposited by e-beam evaporator on the tunnel oxide at room temperature. Then the wafer was transferred into a low pressure chemical vapor deposition (LPCVD) system for VSS Si growth. Typical growth temperature used in our experiment is 600 °C, which is much lower than the eutectic temperature of 979 °C (Ref. 10) between Pt and Si, indicating that the growth mode is VSS rather than vapor-liquid-solid. Si growth rate calibration experiments were carried out in order to control the growth time to avoid the growth of Si NWs and form high-density PtSi NCs for device fabrication. After PtSi NCs were formed, control oxide of 20 nm was deposited in another LPCVD furnace. Finally, Al was evaporated on the front and back of the wafer as contacts of MOS memories.

X-ray photoelectron spectroscopy (XPS) was used to study the chemical nature of the NCs. Figure 2 shows high-resolution XPS data for Pt $4f$ of the sample with the NC average size of 5 nm and density of 1.5×10^{12} cm^{-2} [scanning electron microscopy (SEM) image in the inset of Fig. 2]. The binding energy of Pt $4f$ was obtained at 73.1 and 76.4 eV,[11] indicating the nature of the NCs is PtSi, confirming the Si diffusion into Pt catalysts to form silicide NCs. A reference sample running the same temperature ramping process with this PtSi NCs sample except the introduction of the SiH_4 exhibits Pt NC average size of about 4 nm and the same density as PtSi NCs. The larger size of PtSi NC further confirms the Si growth into Pt catalyst.

Figure 3 shows the capacitance-voltage (C-V) sweep characteristics of PtSi NC MOS memory sample with the dot density of 1.5×10^{12} cm^{-2}. The scanning gate voltage changes from ±2 to ±10 V and the observed memory window increases from 0.26 to 8.2 V, indicating that the memory effect is due to the NC storage rather than defect/interface state charging. C-V sweep experiments of a reference sample without NCs between control and tunnel oxide were also

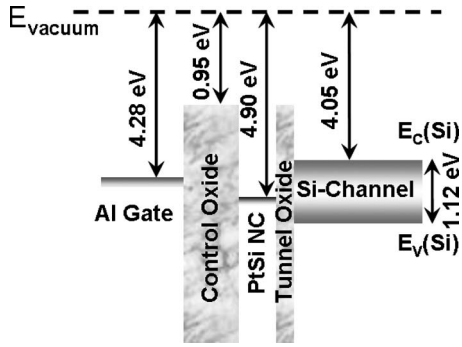

FIG. 1. Energy band diagram of floating gate memory with PtSi NCs. Deep quantum well of 3.95 eV exists between PtSi and SiO_2.

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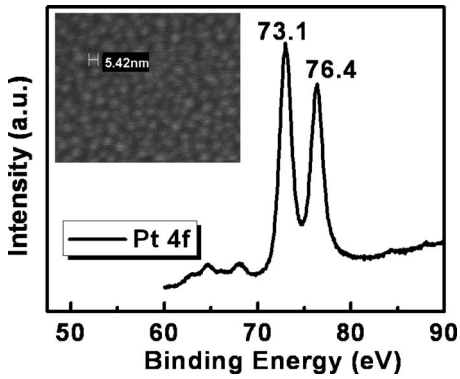

FIG. 2. XPS result of PtSi NCs on SiO_2/Si substrate and Pt $4f$ peak position confirms the chemical nature of NCs is PtSi. The inset is the SEM image of PtSi NCs on SiO_2/Si substrate. The density and average size of PtSi NCs is 1.5×10^{12} cm^{-2} and 5 nm, respectively.

carried out and no hysteresis behavior was found (not shown here). This further confirms the fact that no defect/interface charging contributes to the memory effect, observed in PtSi NC memory.

Figure 4 shows the dependence of flat band voltage (V_{FB}) shift and number of electrons and holes stored in each NC on the programming voltage. The writing of electrons was conducted by biasing a positive voltage, while for programming with holes (erasing), a negative bias was applied on the gate. The charges in a single device is calculated from: $Q=\varepsilon_{SiO_2}/d_{SiO_2}\Delta V_{FB}$, where Q is the charges stored in a MOS device, ε_{SiO_2} is the dielectric constant of SiO_2, d_{SiO_2} is the thickness of control oxide, which is 20 nm in this work, and ΔV_{FB} is the V_{FB} shift between fresh state and programmed/erased state. The charge number per NC is calculated from: Number/dot$=Q/Dq$, where D is the NC density, which is 1.5×10^{12} cm^{-2} here and q is the electron charge. As the programming/erasing voltage increases, the threshold voltage shift and stored charges increase until saturated.

Figure 5 shows retention characteristics of PtSi NC memory at programmed and erased states, respectively. The programming and erasing conditions are gate voltage of 10 V/5 s and −10 V/5 s, respectively. After programming, transient capacitance at the same read voltage is recorded intermittently. After 10^5 s, the charges remained in the NCs at both programmed and erased states are about 70%, which is reasonable for a tunnel oxide of 3 nm. Endurance characteristics of PtSi NC memory is shown in Fig. 6. Two sets of

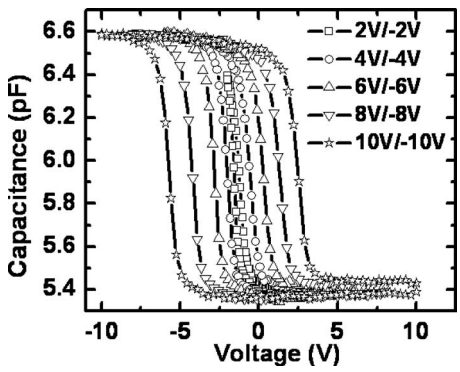

FIG. 3. C-V sweep of MOS memory device with PtSi NCs under different scanning gate voltage from ±2 to ±10 V.

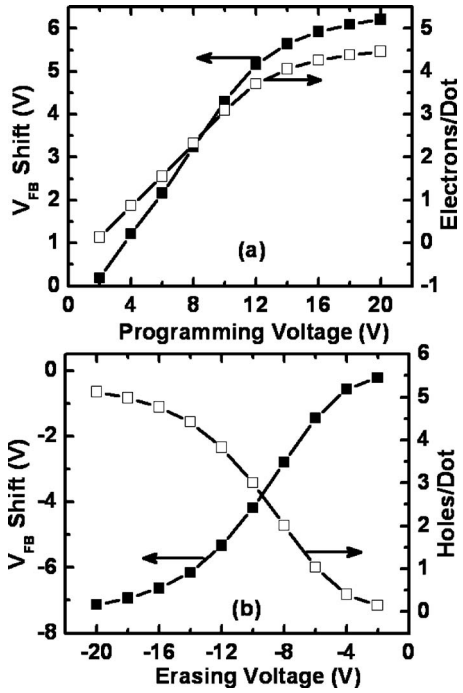

FIG. 4. Plots of flatband voltage shift and corresponding electrons (a) and holes (b) per NC as a function of programming/erasing voltage.

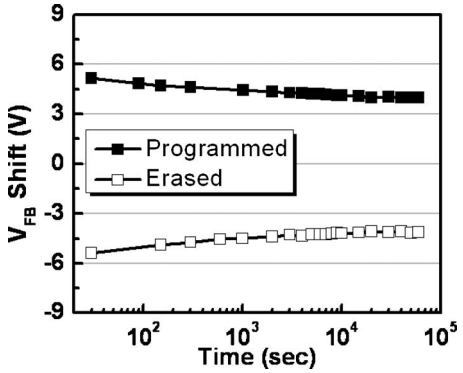

FIG. 5. Retention characteristics of PtSi NC memory at programmed and erased states.

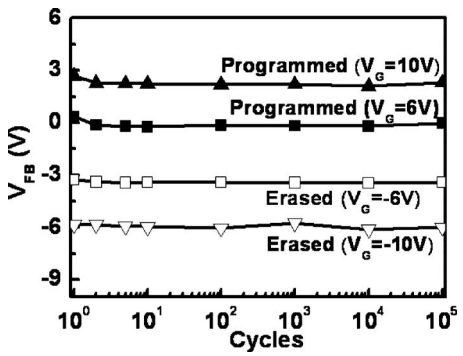

FIG. 6. Endurance performance of PtSi NC memory.

programming/erasing conditions, ±6 and ±10 V, were used to measure the cycling performance. It is found that up to 10^5 times of operation, the memory window, i.e., V_{FB} difference between programmed and erased states, shows insignificant change for both sets of operation.

In summary, VSS mechanism was used to synthesize PtSi NCs with high density and small size. MOS memory with PtSi NCs embedded in SiO_2 was fabricated and characterized. Large memory window, long retention time, and good endurance performance were demonstrated in PtSi NC memory.

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