$CoSi_2$-coated Si nanocrystal memory

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$CoSi_2$-coated Si nanocrystals were fabricated as the floating gates for nonvolatile memory applications to improve the Si nanocrystal memory performance in terms of programming/erasing efficiency and retention time. Discrete $CoSi_2$-coated Si nanocrystals were formed by silicidation of Si nanocrystals on SiO_2 and subsequent selective etching of unreacted metal cobalt over silicide. Metal-oxide-semiconductor field-effect transistor memories with $CoSi_2$-coated Si nanocrystals and reference Si nanocrystals as floating gates were fabricated and characterized. Longer retention, larger charging capability and faster programming/erasing were observed in $CoSi_2$-coated Si nanocrystal memory compared with Si nanocrystal memory. $CoSi_2$ Fermi-level pinning of defect levels plays important role in the device performance enhancement. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3110183]

I. INTRODUCTION

Nonvolatile memories with discrete charge traps are extensively investigated as one of the possible solutions to the scaling limit of flash memory devices. The localized charge in electrically discrete nodes guarantees insensitivity to stress-induced oxide defects and therefore allows for thinner tunnel oxide and faster programming/erasing speed. Moreover drain turn-on effect is suppressed by using nanocrystals as floating gate so that the cell length can be further scaled.

Recently much effort has been made to develop nonvolatile memory devices using nanocrystals, such as Si,[1] Ge,[2] metal,[3–5] and dielectric materials.[6,7] Other novel structures such as double stack of nanocrystals,[8] engineered dielectric tunneling layers,[9,10] and heteronanocrystals[11,12] are also reported with good memory performance. Metal nanocrystal memory has the advantages over semiconductor counterparts in terms of higher density of states around the Fermi level, which is normally aligned in the forbidden gap of Si, leading to larger memory window and stronger coupling between the nanocrystals and the substrate for faster programming. A wide range of metal nanocrystal materials, such as Au, Ni, and W, have been successfully implemented.[13–15] Silicide-based nanocrystals, which have metallic nature of high density of states and high thermal stability, were proposed to improve memory performance.[16] Shortly after these efforts, other groups followed up with their own efforts on silicide nanocrystal metal-oxide-semiconductor (MOS) memories.[17–23] For example, $CoSi_2$ nanocrystals were formed by exposing the $Co/Si/HfO_2/Si$ stacks in an external UV laser.[17] Double-layer $CoSi_2$ nanocrystal MOS memory was formed by evaporating Si/Co/Si trilayer on tunnel oxide followed by rapid thermal annealing.[18]

In this paper, $CoSi_2$-coated Si nanocrystals are used as the discrete charge traps and MOS field-effect transistor (MOSFET) memories are fabricated and characterized. These $CoSi_2$-coated Si nanocrystals were formed by silicidation of Si nanocrystals on SiO_2 and subsequent selective etching of unreacted metal cobalt over silicide, a process which is similar to the fabrication of $TiSi_2/Si$ heteronanocrystals.[16] Nevertheless, there are several advantages of using $CoSi_2$ over $TiSi_2$ in this process. Among all silicides, $CoSi_2$ shows little reactivity with metal/oxide interface.[24] The formation of $TiSi_2$ on Si nanocrystals by annealing is much more difficult and requires much higher temperature due to fine-line effect.[25] Owing to high-density interface states between silicide and Si, the defects induced during original formation of Si nanocrystals may be pinned at the Fermi level of silicide,[26–30] leading to uniform programming/erasing among the devices on a chip. This was not recognized in our earlier $TiSi_2$ nanocrystal memory effort. Furthermore, $CoSi_2$ pins the Fermi level deeper than that of $TiSi_2$, leading to better electron retention. Compared with other methods as discussed earlier, the $CoSi_2$-coated Si nanocrystals approach presents minimized change in the process of Si nanocrystal memories, which are currently pursued by industry for commercialization.

II. EXPERIMENTAL METHODS

A 5 nm thermal oxide was grown on the *p*-Si (100) substrate at 850 °C for 5 min followed by a 900 °C *in situ* annealing in N_2. Si nanocrystals were deposited on the tunnel oxide by low pressure chemical vapor deposition (LPCVD) at 600 °C and 200 mTorr. After the Si nanocrystals deposition the wafer was immediately transferred to another chamber for cobalt sputtering. The thickness of the deposited cobalt film is about 1–2 nm. Two steps of annealing at 600 and 850 °C, respectively, and selective etching of unreacted Co over $CoSi_2$ in the mixture of H_2SO_4 and H_2O_2 were carried out to form $CoSi_2$-coated Si nanocrystals. Then a 20 nm control oxide was deposited at 400 °C by LPCVD followed by undoped poly-Si deposition and patterning. Phosphorous atoms were implanted to form heavily doped gate/source/drain regions simultaneously. Aluminum was evaporated as

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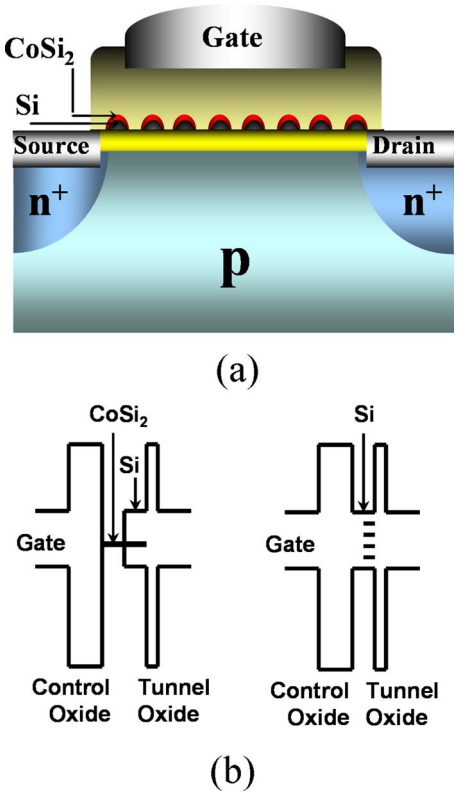

FIG. 1. (Color online) (a) Schematic of $CoSi_2$-coated Si nanocrystal memory device, and (b) energy band diagrams of $CoSi_2$-coated Si nanocrystal and Si only nanocrystal memories. Wide distribution of deep levels arises from embedding of Si nanocrystals in oxide (right schematic). These deep levels may be pinned along the Fermi level of $CoSi_2$ (left schematic).

the contacts to the three terminals. Reference Si nanocrystal memory and a device without floating nanocrystals were also fabricated in the same fabrication run for comparison.

III. RESULTS AND DISCUSSION

Figure 1(a) shows the schematic cross section of $CoSi_2$-coated Si nanocrystal memory. Figure 1(b) shows energy band diagrams for both $CoSi_2$-coated Si nanocrystal memory and Si nanocrystal memory. The wide distribution of defect related deep levels are associated with the Si nanocrystal memory,[31] as depicted in the schematic of Fig. 1(b) in the right. Although the existence of these defects in Si nanocrystals results in relatively long retention performance, this defect-related retention enhancement is not thermally robust.[32] The left one in Fig. 1(b) is the diagram of $CoSi_2$-coated Si nanocrystal memory. The reported work function of $CoSi_2$ is 4.55 eV,[33] namely, the Fermi-level of $CoSi_2$ is within the band gap of Si and close to Si intrinsic Fermi-level. However when $CoSi_2$ connects with Si, the actual Fermi level of $CoSi_2$ is pinned around Si valance band, together with those interface defect states.[26,27] Owing to the pinning effect and high density of states around the Fermi level, $CoSi_2$-coated Si nanocrystal memory can achieve larger storage capacity, more uniform program/erase, and stable retention performance.

The insets (a) and (b) of Fig. 2 show the scanning electron microscope (SEM) images of Si nanocrystals and $CoSi_2$-coated nanocrystals, respectively. The average size of

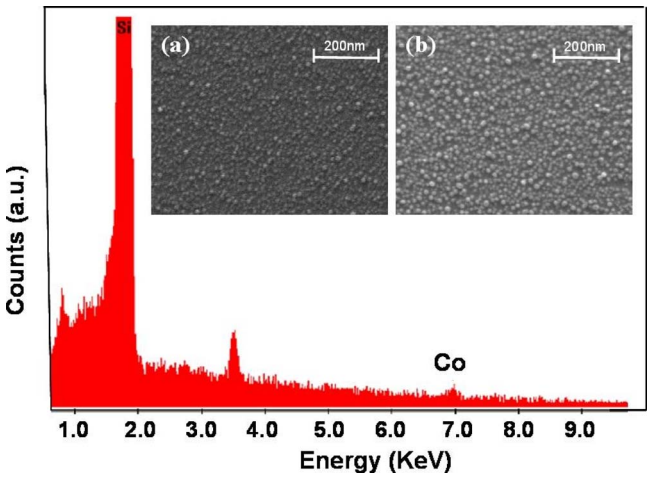

FIG. 2. (Color online) EDX spectrum of $CoSi_2$-coated Si nanocrystals. Insets show the SEM images of (a) Si nanocrystals and (b) $CoSi_2$-coated Si nanocrystals.

Si nanocrystals and $CoSi_2$-coated Si nanocrystals is 10 and 12 nm, respectively, and the density of dots for both Si and $CoSi_2$-coated Si is about 4×10^{11} cm^{-2}, indicating that $CoSi_2$ and Si nanocrystals are well self-aligned. Figure 2 is the energy dispersive x-ray analysis (EDX) spectrum of $CoSi_2$-coated Si nanocrystals. Cobalt signal at 6.9 eV is clearly observed. Because we had a selective etching step in between two annealing steps to have unreacted Co removed, Co signal in the spectrum suggests that $CoSi_2$ is formed and covers the Si nanocrystals.

Si nanocrystal and $CoSi_2$-coated Si nanocrystal MOS memories were fabricated and tested. The tunnel oxide and control oxide thicknesses are 5 and 20 nm, respectively. Figure 3(a) shows high frequency (1 MHz) capacitance-voltage (C-V) sweep of $CoSi_2$-coated Si nanocrystal MOS memory with different scanning range from ±4 to ±10 V. Scanning starts from inversion region to accumulation region and back to inversion region again. Figure 3(b) shows the comparison of normalized C-V sweep at ±10 V between Si nanocrystal and $CoSi_2$-coated Si nanocrystal MOS memories. A larger memory window is observed from $CoSi_2$-coated Si nanocrystal MOS memory, which is due to the large density of states in the metallic $CoSi_2$. For MOS memory without nanocrystals, the flat band voltage shift between programming and erasing is negligible, as shown in Fig. 3(c).

Figure 4 shows the programming and erasing characteristics of Si nanocrystal and $CoSi_2$-coated Si nanocrystal memories. Agilent 81104A Pulse Generator is used to operate the devices and threshold voltage was read from Agilent 4155C Semiconductor Parameter Analyzer. The gate bias of 16 and -16 V were used to program and erase the devices, respectively, and programming and erasing time is accumulated from 2 ns to 10 s. Faster programming/erasing speed is observed in $CoSi_2$-coated Si nanocrystal memory, which can be explained by the stronger coupling between metallic $CoSi_2$ and the channel. $CoSi_2$-coated Si nanocrystal memory also shows a higher level of threshold voltage (V_T) shift saturation, indicating larger storage capability.

Figure 5 shows the endurance characteristics of Si nanocrystal and $CoSi_2$-coated Si nanocrystal memories. The pro-

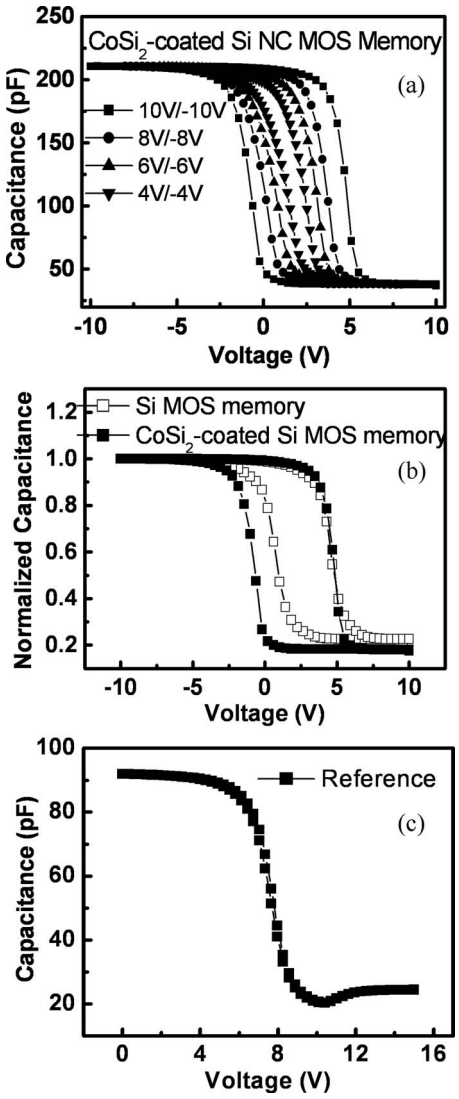

FIG. 3. (a) Capacitance-voltage (C-V) sweep of MOS memory with $CoSi_2$-coated Si nanocrystals, (b) C-V comparison between $CoSi_2$-coated Si nanocrystal and Si nanocrystal memories, (c) C-V sweep of MOS reference device, where no nanocrystals were embedded.

gramming and erasing conditions are ±16 V for 200 ms. The memory windows of the two devices stay open up to 10^5 times of operation, although the magnitude shrinks about 25%. The up-shift in the threshold voltage with times of operation is due to the accumulated trapped positive charges in the oxide layer.

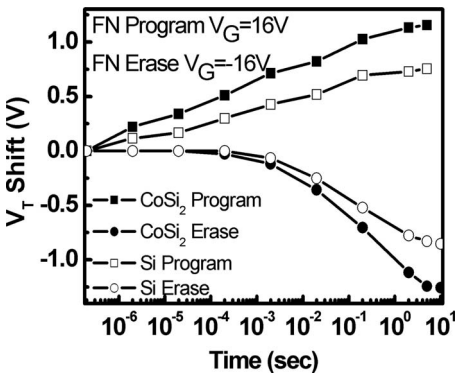

FIG. 4. Transient programming and erasing characteristics of Si nanocrystal and $CoSi_2$-coated Si nanocrystal memories.

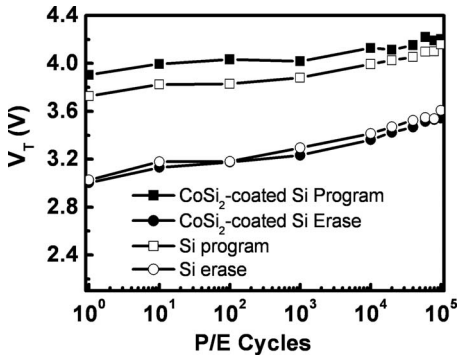

FIG. 5. Endurance characteristics of Si nanocrystal and $CoSi_2$-coated Si nanocrystal memories.

Retention characteristics of Si nanocrystal and $CoSi_2$-coated Si nanocrystal memories are shown in Fig. 6. The plot is the remaining charge percentage converted from the V_T shift against waiting time. $CoSi_2$-coated Si nanocrystal memory demonstrates a longer retention time compared to Si nanocrystal memory. This indicates that $CoSi_2$-coated Si nanocrystals indeed realign their original wide distributed defect-related energy levels around the Fermi-level of the silicide, which is deeper.

To prove the discrete nature of $CoSi_2$-coated Si nanocrystals and the capability of local charge storage, hot carrier injection (HCI) was also used to write electrons onto portions of these nanocrystals near the drain side. Programming and erasing characteristics are shown in Fig. 7. Gate and drain voltage of 7.5 and 5 V were used to charge and −10 and 5 V were used to discharge the devices. Similar to Fowler–Nordheim (FN) operation, device performance enhancement in $CoSi_2$-coated Si nanocrystal memory is observed in terms of faster programming and larger charge capability. Figure 8 shows the retention characteristics comparison between HCI-programmed $CoSi_2$-coated Si nanocrystal and Si nanocrystal memories. Longer retention was observed in $CoSi_2$-coated Si nanocrystal memory and the charge loss after 10^5 seconds in $CoSi_2$-coated Si nanocrystal and Si nanocrystal memories are ~20% and ~38%, respectively. The better retention in $CoSi_2$-coated Si nanocrystal memory can be attributed to the primarily charging around the silicide Fermi-level instead of the defect levels in Si nanocrystals due to the Fermi-level pinning effect. Figure 9 shows the threshold voltage shift as a function of waiting

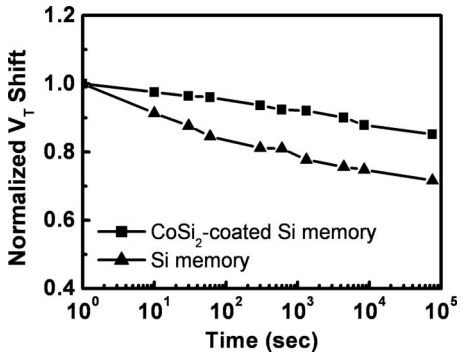

FIG. 6. Remained charge percentage converted from threshold voltage shift as a function of time.

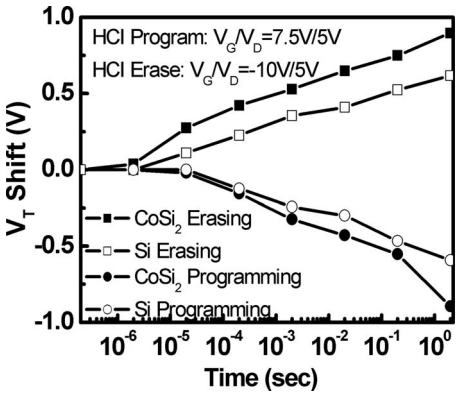

FIG. 7. Hot-carrier programming and erasing characteristics of $CoSi_2$-coated Si nanocrystal and Si nanocrystal memories.

time after the $CoSi_2$-coated Si nanocrystal memory device was programmed at $V_G/V_D=7.5/5$ V for 2 s. Forward (read from drain) and reverse (read from source) read at different read voltages were used. Because of the local charge storage near the drain side, an additional energy barrier was formed for channel electrons. When the device was read from the drain (forward), this barrier was effectively lowered at larger read drain voltages, leading to different threshold voltage shift. On the other hand, when the device was read from the source (reverse), the source voltage cannot effectively change this barrier, leading to insignificant change in threshold voltage. This result suggests that the device has the potential to be used for dual-bit application.

IV. SUMMARY

In summary, MOSFET memory devices with $CoSi_2$-coated Si nanocrystals as floating gates were fabricated and characterized. Memory performances between $CoSi_2$-coated Si nanocrystal memory and Si only nanocrystal memory were compared. Better performance in terms of longer retention time, faster operation speed and larger memory window has been achieved in $CoSi_2$-coated Si nanocrystal memory. The Fermi-level pinning as a result of $CoSi_2$ coating results in the device performance enhancement. The work suggests that the simple silicidation treatment of Si nanocrystals may fundamentally solve nonuniform device

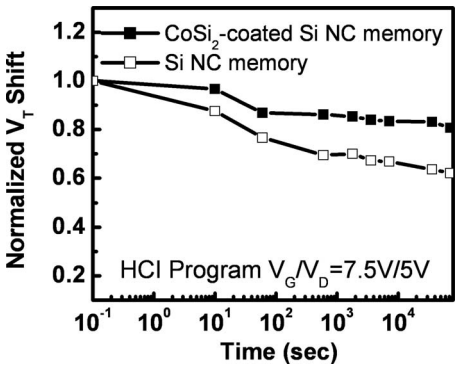

FIG. 8. Retention characteristics of $CoSi_2$-coated Si nanocrystal and Si nanocrystal memories after HCI programming. The charge loss after 10^5 seconds in $CoSi_2$-coated Si nanocrystal and Si nanocrystal memories are ~20% and ~38%, respectively.

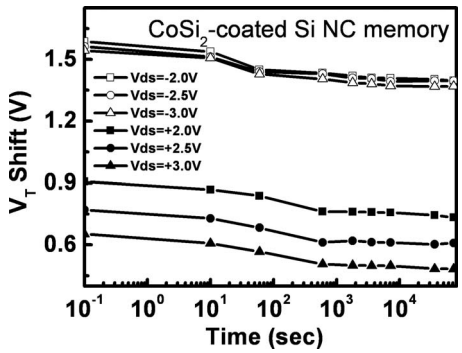

FIG. 9. Retention characteristics of $CoSi_2$-coated Si nanocrystal memory after HCI programming under forward and reversed read conditions.

operation due to the wide distribution of defect levels in Si nanocrystals and allow Si nanocrystal memory to scale further into next nonvolatile memory generations.

ACKNOWLEDGMENTS

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