A $TiSi_2$/Si Heteronanocrystal Memory Operated With Hot Carrier Injections

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***Abstract*—The programming and erasing of a $TiSi_2$/Si heteronanocrystal memory were carried out by channel hot electron injection and drain side hot hole injection, respectively. Compared to an Si nanocrystal memory, a $TiSi_2$/Si heteronanocrystal memory exhibits much better writing/erasing efficiency and higher writing/erasing saturation level. The retention transient process indicates that the $TiSi_2$/Si heteronanocrystal memory has a very slow charge loss mechanism. The result of the localization of charge shows that a reverse read leads to a higher threshold voltage shift, which is almost not dependent on the amplitude of the read voltages.**

***Index Terms*—Flash memory, heteronanocrystal, nonvolatile memory, self-aligned, silicide.**

I. Introduction

FLASH memory devices with localized charge storage nodes, such as Si-oxide-nitride-oxide-Si (SONOS) [1]–[3] and nanocrystal memory devices [4]–[8] attracted much attention recently because of their potential application in future nonvolatile memory technology. The localized charge storage enables the implementation of thinner tunnel oxide for higher programming speed and better device reliability. The discrete nature of charge storage nodes also leads to the concept of dual-bit memory device, in which charges are written to the storage nodes near the drain and/or source sides with channel hot electron injection. This scheme doubles storage density with simple modification of read scheme [9]–[11], and therefore, becomes very promising. Nevertheless, the application of both SONOS and nanocrystal memories for dual-bit scheme remains challenging. For SONOS devices, the erasing saturation and vertical charge immigration are found to be the main concerns [1], [2]. For semiconductor nanocrystal memory devices, Shi's model [12] suggested that traps originating from structural imperfection play a determinant role in charge storage; however, they are thermally unstable. Although metal nanocrystals have deeper confinement levels as a result of their work function and high density of states near Fermi levels, the metal/oxide reaction during annealing is an issue [13]–[15]. Recently, we reported self-aligned $TiSi_2$/Si heteronanocrystal memory devices [16], [17] that can avoid those drawbacks. Compared with Si nanocrystal memory, silicide/Si heteronanocrystal memories possess significantly improved programming and erasing under the Fowler–Nordheim (F-N) tunneling regime. To explore potential applications of silicide/Si heteronanocrystal memory as dual-bit storage cell, in this paper, device performance under channel hot electron injection and drain side hot hole erasing, instead of F-N tunneling, is reported.

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II. Device Fabrication

The process to fabricate MOSFET memories with $TiSi_2$/Si heteronanocrystal floating gate was described elsewhere [17]. Briefly, $TiSi_2$/Si heteronanocrystals were fabricated with two-step self-aligned silicidation technique on 5-nm-thick nitridized tunnel oxide. In the first step, Si nanocrystals were grown at 600 °C for 10 s with the SiH_4 pressure of 136 mtorr in a low-pressure chemical vapor deposition system (CVD). The fabricated Si nanocrystals have an average dot diameter of $\sim$11 nm and a dot density of $\sim 5 \times 10^{11}\text{cm}^{-2}$, characterized by atomic force microscope. Some of these wafers were subjected to the fabrication of Si nanocrystal reference devices while others went to the next step (the second step) for silicide/Si heteronanocrystal fabrication, followed by the heteronanocrystal devices fabrication. The average heteronanocrystal size is 13 nm and the density is also $\sim 5 \times 10^{11}\text{cm}^{-2}$. Control oxide of about 15 nm was then deposited, followed by a 350-nm-thick polysilicon using CVD techniques. The gate/source/drain regions were heavily implanted with phosphorus followed by dopant activation. The final device with aluminum contact possesses a channel length of 1 μm. The devices were characterized with Agilent 4155 C semiconductor parameter analyzer and Agilent pulse generator.

III. Results and Discussion

Fig. 1 shows the writing and erasing characteristics of a $TiSi_2$/Si heteronanocrystal memory and a reference Si nanocrystal memory with channel hot electron injection and hot hole injection, respectively. The hot electron injection scheme is shown as the bottom inset in Fig. 1. Writing was carried out under $V_g = 9$ V and $V_d = 5$ V. After a writing time of 1 ms, the $TiSi_2$/Si heteronanocrystal memory achieves a V_{th} shift of 0.95 V while it is only 0.65 V for Si nanocrystal memory. No evident writing saturation is observed yet for $TiSi_2$/Si heteronanocrystal memory even if the writing time exceeds 30 ms, which might be due to the large charge storage capacity of the metallic silicide. For Si nanocrystal memory, however, writing is saturated after 30 ms.

In erasing operations, the devices were first programmed with $V_g = +9$ V and $V_d = 5$ V for 1 ms, and then erased with hot hole injection with $V_g = -10$ V and $V_d = 5$ V. The hot hole injection scheme is shown as the top inset in Fig. 1. Under this erasing condition, electron band-to-band tunneling occurs and holes are

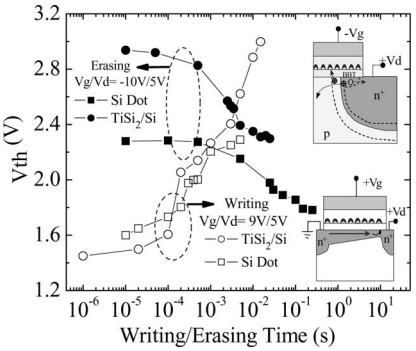

Fig. 1. Writing and erasing characteristics of the $TiSi_2/Si$ heteronanocrystal memory and the reference Si nanocrystal memory. The writing and erasing were carried out with channel hot electron injection and hot hole injection, respectively. The insets are the diagrams of hot electron injection in the writing (bottom) and hot hole injection in the erasing mode (top).

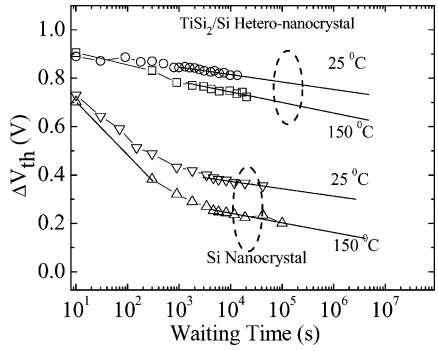

Fig. 2. Retention characteristics of the $TiSi_2/Si$ heteronanocrystal memory and the Si nanocrystal memory at room temperature (25 °C) and high temperature (150 °C).

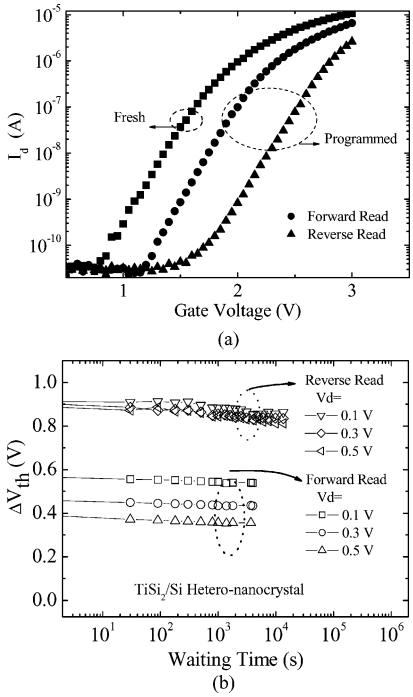

Fig. 3. (a) I_d–V_g curves for both fresh and programmed devices. (b) Retention characteristics of the $TiSi_2/Si$ heteronanocrystal memory under forward read and reverse read schemes and different read voltages.

generated. Some of the holes become hot in the depletion region of a reverse- biased "diode" near drain and are redirected to the nanocrystals by negative gate voltage to neutralize the electrons. As shown in Fig. 1, the heteronanocrystal memory has a faster erasing speed than the Si nanocrystal memory. It takes 0.25 s for the Si nanocrystal memory to achieve a $\Delta V_{\rm th}$ of -0.5 V. On the contrary, it is only 4.8 ms for the $TiSi_2/Si$ heteronanocrystal memory to achieve the same $\Delta V_{\rm th}$.

The much improved writing/erasing performances in the heteronanocrystal memory can be understood as follows. The metallic silicide layer of the heteronanocrystal acts as trapping layer with very high trap density, leading to a much higher charge capture capability than an Si nanocrystal. Therefore, the $TiSi_2/Si$ heteronanocrystal memory exhibits larger $\Delta V_{\rm th}$. In addition, silicide/Si heteronanocrystals have less Coulomb blockade effect than Si nanocrystals due to their metallic nature. Furthermore, the metal silicide part deforms the electric field and enhances the potential coupling from the control gate to the dot [18]. The deformed potential distribution helps the capture of injected carriers (electrons or holes). Accordingly, the $TiSi_2/Si$ heteronanocrystal memory has a faster writing speed. The observed faster erasing speed and higher erasing saturation of the $TiSi_2/Si$ heteronanocrystal memory over Si nanocrystal memory can be readily understood because the main erasing process here is hot hole "writing" process to neutralize the electrons in the floating gate. Therefore, the reasons for faster electron writing speed and higher writing saturation analyzed earlier also apply for the hole writing process in the erasing operation.

The retention transient characteristics at room temperature (25 °C) and high temperature (150 °C) are shown in Fig. 2 for the memory devices with $TiSi_2/Si$ heteronanocrystals and Si nanocrystals, respectively. The two memory devices were programmed with the combination of $V_g = +9$ V and $V_d = +5$ V for 1 ms. The read operation was done with $V_d = 0.5$ V in the reverse read mode (read from source side). It is evident that the $TiSi_2/Si$ heteronanocrystal memory has a significantly slower charge loss rate than the Si nanocrystal memory at the initial stage. By extrapolating the retention curve, one can expect a memory window of 0.71 V (81% of the initial window) after 10 years of waiting at room temperature for the $TiSi_2/Si$ heteronanocrystal memory. For the Si nanocrystal memory, however, the memory window is 0.23 V (35% of the initial window) after only 1.7×10^4s (4.7 h) because of the large amount of shallow traps in Si nanocrystals [12]. These shallow traps have much higher emission rates than that from the extra quantum well formed by the control oxide/$TiSi_2/Si$ of heteronanocrystal memory. Therefore, the Si nanocrystal memory possesses worse charge retention characteristics than $TiSi_2/Si$ heteronanocrystal memory. The faster charge losses at high temperature (150 °C) for both devices are caused by the enhanced thermal activation rate from the trap sites at high temperature. Nevertheless, since most charges are stored in the silicide region in the $TiSi_2/Si$ heteronanocrystal memory, it depends much less on temperature than the Si nanocrystal memory.

To investigate dual-bit capability of our heteronanocrystal memory, we carried out retention characteristics under both forward and reverse read schemes. In Fig. 3(a), the I_d–V_g curves exhibit evident difference in electrical characteristics under forward and reverse read modes. The results in Fig. 3(b) suggest that $\Delta V_{\rm th}$ is sensitive to V_d in the forward read scheme while it is almost constant in the reverse read mode under different read voltages. Since the charges are mostly stored in the nanocrystals near the drain side, the bias condition at the source side (reverse read mode) will not significantly influence the $V_{\rm th}$. Only when read voltage is applied to the drain side, $V_{\rm th}$ is remarkably dependent on the read voltage V_d because the barrier for the carriers can be readily adjusted by the read voltages.

IV. Conclusion

The device performances of a MOSFET memory with $TiSi_2$/Si heteronanocrystal floating gate were investigated with channel hot carrier injections. Compared with the Si nanocrystal memory, the $TiSi_2$/Si heteronanocrystal memory exhibits faster programming/erasing speed, higher saturation level, and remarkably better retention performance. Compared with the forward read mode, the threshold voltage shift is larger and depends much less on the read voltages in the reverse read mode. Therefore, the $TiSi_2$/Si heteronanocrystal is a promising candidate to replace the Si nanocrystal for the next-generation floating gate flash memory devices with dual-bit per cell function.

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