Transport property of Si/Si$_{1-x}$Ge$_x$/Si *p*-type modulation doped double heterostructure

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(Received 7 January 1994; accepted for publication 22 April 1994)

High mobility Si/Si$_{1-x}$Ge$_x$/Si *p*-type modulation-doped double heterostructures with Ge fractions of 0.2, 0.25, 0.3 have been grown by rapid thermal process/very low pressure-chemical vapor deposition. Hole Hall mobilities as high as $\sim$300 cm^2/V s (at 293 K and sheet carrier concentration of $\sim 2.6\times 10^{13}$ cm^{-2}) and $\sim$8400 cm^2/V s (at 77 K and sheet carrier concentration of $\sim 1.2\times 10^{13}$ cm^{-2}) have been obtained for heterostructures with $x=0.3$. The variation of hole mobility with temperature and the influence of the Ge fraction on hole mobility were investigated.

In recent years, the Si/SiGe modulation doped (MD) heterostructures have created a great deal of interest for fundamental investigations and for high speed device applications (modulation doped field-effect devices). High hole mobility *p*-Si/SiGe MD heterostructure[1–4] and high electron mobility *n*-Si/SiGe MD heterostructure[1,5] have been reported.

In this communication, we report that Si/Si$_{1-x}$Ge$_x$/Si *p*-type modulation doped double heterostructures have been grown by rapid thermal process/very low pressure-chemical vapor deposition (RTP/VLP-CVD).[6] The electrical properties were measured and analyzed. The variation of hole mobility with temperature and the influence of the Ge fraction on hole mobility were investigated.

Si/Si$_{1-x}$Ge$_x$/Si modulation-doped double heterostructure samples were grown in a computer controlled RTP/VLP-CVD system. As shown in Fig. 1(a), the *i*-Si buffer layers (150 nm), p^+-Si doped layers (20 nm), *i*-Si spacer layers (15 nm), undoped Si$_{1-x}$Ge$_x$ strained layers (40 nm), *i*-Si spacer layers (15 nm) and p^+-Si doped layers (20 nm) were epitaxially grown orderly on (100) p^--Si substrates. The Ge fractions of x were selected to be 0.2, 0.25, and 0.3. The dopant concentration of boron doped p^+-Si layer was $1-3\times 10^{19}$ cm^{-3}. The epitaxy was carried out at a temperature of 600 °C with SiH$_4$, GeH$_4$, and B$_2$H$_6$ as the gas sources. Before growth, the samples were hot cleaned and preprocessed with hydrogen, to obtain high quality single crystal Si layers and SiGe strained layers. In the design of the sample structure, the thickness of the spacer layer is very important. Considering the additional potential field range of ionized impurities and the segregation width of boron and germanium, the thickness of spacer layer was designed to be 15 nm.

Figure 1(b) is the energy band diagram for MD sample. Because the band gap offset for Si/SiGe heterojunction is presents mainly the valence band,[7] hole potential wells are formed on the SiGe side of the Si/SiGe interface and carriers in the p^+-Si layer will be transferred to the SiGe potential wells, thus forming a two dimensional hole gas (2DHG).

In order to compare the transport properties, uniformly doped (UD) samples were also grown under the same conditions, the Si$_{0.3}$Ge$_{0.2}$ layer of 180 nm thickness was doped with boron to $1-3\times 10^{19}$ cm^{-3}, which was the same as the dopant concentration of p^+-Si layers of MD samples.

Both the MD and UD samples were measured by the conventional Hall–van der Pauw method, in which a lock-in ac measurement was used to reduce secondary action. The temperature range for measurement was 77–293 K.

The Hall data are listed in Table I. It can be seen that the hole Hall mobilities for both the UD bulk Si sample (No. 5) and the Si/SiGe sample (No. 4) are lower at 77 K than at room temperature. This is caused mainly by the ionized impurities scattering at low temperature.

At room temperature, the hole Hall mobilities of MD samples (Nos. 1–3) are 240–300 cm^2/V s, which are many times higher than the bulk Si sample and also a little higher than UD sample No. 4, The primary reason is that the hole effective mass in Si$_{1-x}$Ge$_x$ is smaller than Si. Although there is alloy disorder scattering in the SiGe layer, the influence is negligible,[8] while at low temperature, the hole mobilities of all the MD samples increase greatly. For sample No. 3 ($x=0.3$), the hole Hall mobility reaches 8400 cm^2/V s at 77 K. This clearly indicates that the carriers (holes) of MD samples are transferred from the parent impurities of the p^+-Si layer

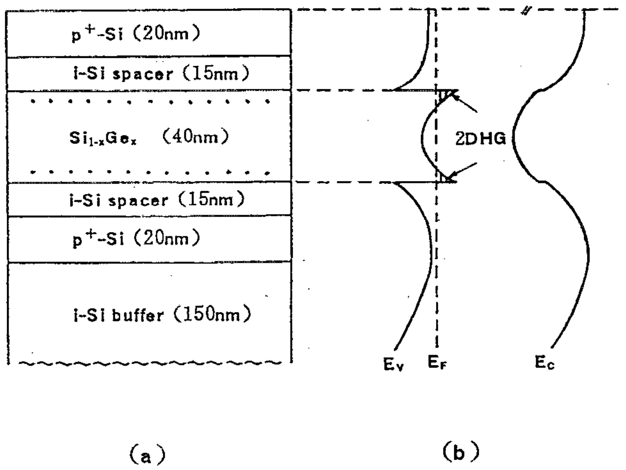

FIG. 1. Schematic for Si/Si$_{1-x}$Ge$_x$/Si *p*-type modulation-doped double heterostructure (a) and the corresponding energy band diagram (b).

0021-8979/94/76(4)/2544/3/$6.00

TABLE I. Hall data for MD and UD samples at 293 and 77 K.

Sample No.	Ge fraction	MD/UD	p_s ($\times 10^{13}$ cm^{-2}) 293 K	p_s ($\times 10^{13}$ cm^{-2}) 77 K	μ_h (cm^2/V s) 293 K	μ_h (cm^2/V s) 77 K
1	(x=0.2)	MD	6.6	2.2	240	5300
2	(x=0.25)	MD	6.7	2.3	280	7500
3	(x=0.3)	MD	2.6	1.2	300	8400
4	(x=0.2)	UD	6.5	7.3	210	130
5	(x=0)	UD	2.1×10^{19} cm^{-3}	3.1×10^{19} cm^{-3}	38	26

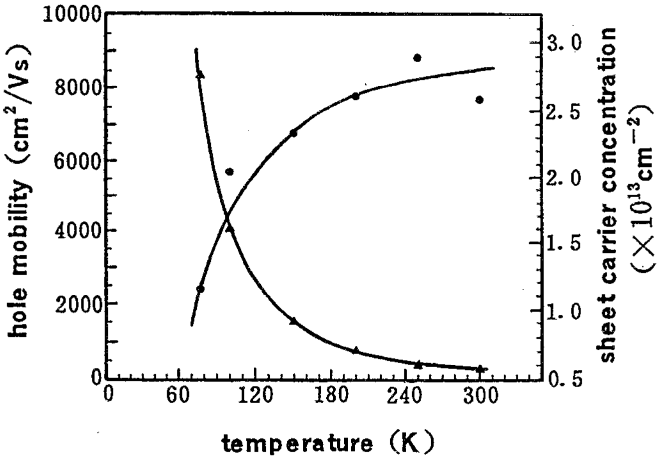

FIG. 2. Temperature dependence of hole Hall mobility and sheet carrier concentration for Si/Si$_{0.7}$Ge$_{0.3}$/Si p-type modulation-doped double heterostructure.

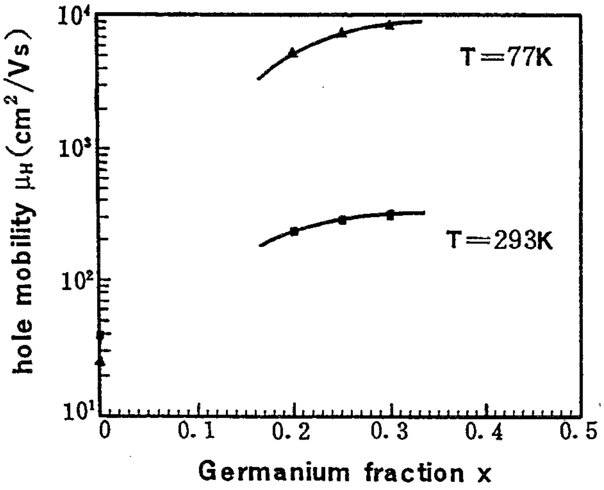

FIG. 3. Hole Hall mobility vs Ge fraction at 293 and 77 K for Si$_{1-x}$Ge$_x$/Si p-type modulation-doped double heterostructure.

to the undoped SiGe channel and the remote ionized impurity scattering is greatly reduced.

Figure 2 shows the temperature dependence of hole Hall mobility and sheet carrier concentration for a typical MD sample (x=0.3). The hole mobility increases with the decrease of temperature, because the lattice scattering decreases with decreasing temperature, and the influence of remote ionized impurities scattering is very small. The decrease of sheet carrier concentration at low temperature indicates that some of the holes have been frozen.

The dependence of hole mobilities on the Ge fraction (x) for MD heterostructures at room temperature (293 K) and low temperature (77 K) is shown in Fig. 3. The mobilities increase with increasing x. At room temperature, the scattering mechanism consists primarily of lattice scattering and alloy scattering. With increasing x, the hole effective mass decreased and hole mean free time increased, although the alloy disorder scattering increased with increasing x, the influence was small, so the hole mobility tended to increase. This is in accordance with the results of theoretical calculations.[8] At low temperature the hole mobilities increased with increasing x; this was induced primarily by the decrease of the hole effective mass.

The mobility in SiGe MD heterostructures depends strongly upon the lattice integrity of the SiGe alloy layers and Si/SiGe interfaces. Misfit dislocation, background impurity scattering, and interface roughness scattering will reduce the mobility, especially at low temperature.[9] The high hole mobilities achieved for our samples both at room and low temperature (77 K) are evidence of high quality SiGe strained layers and Si/SiGe interfaces.

Sheet carrier concentration p_s is another important value in Hall measurement, which depends primarily upon dopant concentration, the thickness of the spacer layer, and the crystal quality of structure material. The product of u_H and p_s is an essential parameter for evaluating the quality of high speed field effect devices. The sheet carrier concentrations of our MD samples are all higher than 1×10^{13} cm^{-2} and the values reported so far.[1-4]

In conclusion, Si/Si$_{1-x}$Ge$_x$/Si p-type MD double heterostructure with high hole mobilities and high sheet carrier concentration has been achieved by RTP/VLP-CVD. The hole Hall mobilities as high as ~300 cm^2/V s (293 K, p_s~2.6×10^{13} cm^{-2}) and ~8400 cm^2/V s (77 K, p_s~1.2×10^{13} cm^{-2}) for x=0.3 are the highest values reported so far. Experiments showed that the hole mobility was apparently enhanced with decreasing temperature and increased with increasing Ge fraction.

The authors gratefully acknowledge the 301 group of Nanjing Electronic Devices Institute for Hall measurements, the colleagues of our research group, and Gao Weizhong and Li lianzhu for their valuable discussion and technical assistance.

[1] Y. H. Xie, E. A. Fitzgerald, D. Monroe, P. J. Silverman, and G. P. Watson, J. Appl. Phys. **73**, 8364 (1993).

[2] P. J. Wang, B. S. Meyerson, F. F. Fang, J. Nocera, and B. Parker, Appl. Phys. Lett. **55**, 2333 (1989).

[3] D. J. Gravesteijn, T. Mishima, C. W. Fredriksz, G. F. A. van de Walle, and R. A. van den Heuvel, J. Cryst. Growth **111**, 916 (1991).

[4] V. Venkataraman, P. V. Schwartz, and J. C. Sturm, Appl. Phys. Lett. **59**, 2871 (1991).

[5] F. Schaffler, D. Tobben, H. J. Herzog, G. Abstreiter, and B. Hollander-,Semicond. Sci. Technol. **7**, 260 (1992).

[6] Z. Youdou, Z. Rong, J. RuoLian, H. Liqun, Z. Peixing, M. Shuiyuan, Y. Shidong, L. Qi, and F. Duan, *Proceedings of 20th International Conference on the Physics of Semiconductors* (World Scientific, Thessaioniki, Greece, 1990), Vol. 2, p. 869.

[7] R. Dingle, H. L. Störmer, A. C. Grossard, and W. Weigmann, Inst. Phys. Conf. Ser. **45**, 248 (1979).

[8] T. Manku and A. Nathan, IEEE Electron Device Lett. **12**, 704 (1991).

[9] A. Gold, Phys. Rev. B **35**, 723 (1987).