I. INTRODUCTION

Silicon quantum wires (SQWRs) can play an important role in ultralarge scale integration (ULSI) and high performance quantum effect devices. Moreover, the band structure of artificially modulated silicon nanostructures is different from that of bulk silicon, which would make it possible to obtain novel optical and electronic properties and to apply them in silicon-based optoelectronic integrated devices. Hence, there has been great interest in developing techniques to fabricate SQWRs in recent years. Up to now, most of quantum wires have been made by fabricating a grating-like gate on top of a two-dimensional electron gas contained in a semiconductor heterojunction or in metal–oxide semiconductor structures. By applying a negative gate voltage, the system can be changed from the two- to one-dimensional regime, where electron confinement is achieved by an electrostatic confining potential. However, only few methods have been developed to obtain ultrafine SQWRs and establish one-dimensional confinement by physical boundaries. The thermal oxidation method was used on thin silicon columns to form silicon nanostructures: this may present a method of fabricating fully contained SQWRs with SiO2 acting as a high potential barrier. The fabrication of an array of SQWRs with SiO2/Si interfaces laying on silicon substrate by anisotropic wet chemical etching and thermal oxidation was reported. Also, a silicon single electron transistor operating at room temperature was studied by controlling the structure of a wire-patterned very thin silicon layer through pattern-dependent oxidation. At the present stage, obviously, it is necessary to develop advanced fabrication techniques to obtain high quality ultrafine SQWRs.

II. EXPERIMENTAL PROCEDURE

In this work, (100)-oriented p-type silicon wafers with resistivities of 25–50 Ω cm were used as substrates. The SiGe/Si heterostructure film was grown by very low pressure chemical vapor deposition (VLP-CVD) using SiH4 and GeH4 as the source gases. Details of the growth technique have already been reported elsewhere. A 100-nm-thick silicon buffer layer was grown on the silicon substrate prior to the growth of the SiGe layer. The Si0.8Ge0.2 layer was grown between the buffer layer and the superficial silicon layer.
Subsequent mask and lithography techniques were carried out to generate line-and-space patterns on the Si/SiGe/Si heteroepitaxial film. Then trenches were formed by reactive ion etching using SF$_6$ gas. Next the selective chemical etchant consisting of HNO$_3$:CH$_3$COOH:diluted HF solution at 25 °C was used to etch the trench structures to remove the Si$_{0.8}$Ge$_{0.2}$ layer and retain the silicon wires. After removing the mask, the as-etched silicon wires were thermally oxidized in a wet oxygen atmosphere, which smoothes the surface of the silicon wires and reduces the lateral dimensions to produce the expected ultrafine SQWRs. Finally, thermal oxidation in dry oxygen was carried out to obtain high-quality Si/SiO$_2$ interfaces.

For investigating the fabrication progression of SWQs, the cross sections of the fabricated SQWRs were observed by SEM. In order to clearly distinguish the SQWRs, a sample was deposited on a polysilicon film mask on the SQWRs by the VLP-CVD reactor, and then was backside polished and cleaved. The cleaved faces were etched with a diluted HF for several minutes. This facilitated the differentiation between the SQWR and the oxide. The space vacated by the oxide now appears like a dark strip sandwiched between two bright areas of silicon and polysilicon. A thin layer of gold was then sputter deposited onto the exposed face to alleviate sample charging. These procedures provided excellent contrast in the SEM image. Dimensional data measurements were taken manually from SEM photographs.

III. RESULTS AND DISCUSSIONS

A. SiGe/Si heteroepitaxy

From Fig. 1, it can be noted that the whole fabrication process is based on SiGe/Si heterostructures. Therefore, realization of high-quality SiGe/Si heteroepitaxial films with abrupt interfaces is a prerequisite for fabricating ultrafine SQWRs. Figure 2 shows the temperature dependence of the growth rates of Si and SiGe alloys on the Si(100) substrate. In the present work, the growth temperature is at 600 °C, and the growth rate level is 1 s, which offers the capability of controlling atomically precise thicknesses and abrupt interfaces. An advantage of this type process is that the expected thickness of the superficial silicon layer can be easily achieved, which is important for controlling the lateral dimensions of the SWQs. In general, decreasing the mole fraction of Ge in the SiGe alloy is beneficial in obtaining high-quality heteroepitaxial films, whereas it is not good to have high selectivity in the chemical etching. Hence, the optimum mole fraction of Ge is selected as 0.2. Here, the thickness of Si$_{0.8}$Ge$_{0.2}$ layer is below the critical thickness for the introduction of misfit dislocations, and the Si$_{0.8}$Ge$_{0.2}$ layer is pseudomorphically strained.

B. Selective chemical etching

In the last several years, selective chemical wet etching techniques for SiGe/Si heteroepitaxial films have been devel-
oped. The characteristics of several selective chemical etchants were investigated, and it was demonstrated that HNO$_3$ : CH$_3$COOH : diluted HF was very good in reducing SiGe nanostructures. Furthermore, the advantages of this etchant for the present fabrication process are that it is compatible with the mask and lithography processes, and the optimum etch rate and selectivity are easily obtained by altering the composition. Here, because the linewidth of the mask pattern is wider than the thickness of the superficial silicon layer, the etch rate for silicon is controlled within a value in order to form the silicon wire having a quasisquare cross section. Through selective chemical etching, the Si$_{0.8}$Ge$_{0.2}$ layer is removed and the superficial silicon layer is narrowed to form a silicon wire. Figure 3 shows a cross-sectional SEM image of a silicon wire prepared by selective chemical etching. The top layer above the silicon wire is the mask. The SEM shows a smooth and pit-free surface.

C. Thermal oxidation

Advantages of using dry thermal oxidation to fabricate controllable SQWRs have been demonstrated previously. Self-limiting oxidation phenomena related to viscous oxide stress in silicon nanostructures have been observed. It was seen as an opportunity for producing silicon nanostructures with ±1 nm control in lateral dimensions in the self-limiting regime of oxidation temperatures below 950 °C. For the SiGe/Si heterostructure, however, oxidation at high temperatures above 850 °C is forbidden because of the thermal stability of SiGe alloy, and the dry oxidation at low temperatures is not practical due to taking too long to narrow the silicon wires to the desired lateral dimensions. Fortunately, wet oxidation at low temperatures offers a good opportunity for realizing ultrafine SQWRs. Therefore, two steps of wet and then dry oxidation are carried out; the latter is used to obtain high-quality Si/SiO$_2$ interfaces. Figure 4 shows the cross-sectional SEM image of a SQWR embedded in the oxide after thermal oxidation. Here, the radius of the SQWR is about 20 nm.

Obviously understanding of the wet oxidation of silicon wires is important for fabricating well-controllable ultrafine SQWRs. It is hoped that the self-limiting oxidation effect observed in dry oxidation would also occur in wet oxidation. For that reason, investigation of the characteristic of wet oxidation at three temperatures of 850, 800, and 750 °C were performed. Figure 5 shows that the radii of silicon wires reduce with oxidation time at 850 and 750 °C, respectively. The starting radius of as-etched silicon wires is about 120 nm. As the wet oxidation progresses, oxidation retardation of silicon wires is observed at these temperatures. The oxidation retardation of silicon wires depends strongly on the oxidation temperature, as expected, which is more pronounced at a lower temperature. The final radius seems to self-limit to about 20 nm here. In the case of oxidation at 850 and 800 °C, however, the silicon wires disappear after 16 and 20 h, respectively. On the other hand, it is found that the flat surface oxidizes faster than do silicon wires. As oxidation proceeds, the oxide thickness of the flat surface continues to increase linearly with time while the oxide thickness of silicon wires
Fig. 6. Oxide thickness on SQWR surfaces normalized to that on the flat surface as a function of the inverse of the radius of the SQWs for 850 °C, 800 °C, and 750 °C wet oxidation, respectively.

increases slightly. This oxidation retardation becomes severe by decreasing the radii of the silicon wires. Figure 6 clearly demonstrates the radius and temperature dependence of the retardation, where the vertical axis is the oxide thickness on the silicon wire surfaces normalized to that on the flat surface, and the horizontal axis denotes the inverse of the radius of the silicon wires after oxidation. The characteristic, as shown in Fig. 6, is similar to observations reported previously.\textsuperscript{6,14} Oxidation retardation can usually be attributed to additional stress from nonplanar viscous deformation of the oxide.\textsuperscript{14} Since the molecular volume of SiO\textsubscript{2} is two times larger than the atomic volume of Si, the newly formed oxide expands and pushes out the old oxide. Owing to the very high viscosity of the oxide, nonplanar two-dimensional viscous deformation of the oxide produces large additional stress. This viscous stress makes the oxidation reaction at the silicon surface more difficult. Based on these observations, it is apparent that the extent of oxidation retardation follows the change in viscous stress with the oxidation temperature and the radius of the silicon wires. The temperature dependence of the retardation is mainly associated with that of the oxide viscosity. The viscosity becomes higher at lower temperatures and the stress increases and, consequently, leads to more retardation. In addition, it should be noted that the self-limiting oxidation phenomenon in the present wet oxidation is found to occur only for a temperature of about 750 °C, which is about 200 °C lower than that in dry oxidation.\textsuperscript{6}

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This may be due to the fact that the viscous stress of wet oxide is lower than that of dry oxide. The more severe retardation for smaller radii is the result of higher stress produced by a more drastic deformation of the oxide. For the silicon wire with a smaller radius, the old oxide layer has to expand more to accommodate a given increase in volume for each subsequent reaction; therefore, this causes greater stress normal to the interface, retarding further oxidation. There are two likely mechanisms for explaining the influence of viscous stress on oxidation retardation. One is that the surface reaction coefficient \( K_s \) is reduced by the normal viscous stress at the Si-SiO\textsubscript{2} interface.\textsuperscript{14} Another is that oxidation diffusion is limited in a highly stressed oxide.\textsuperscript{15} Up to now, there are still insufficient data to construct a unique predictive model to explain all the oxidation phenomena associated with silicon nanostructures. Further studies are needed to identify the effects of the viscous stress on oxidation kinetic parameters. From the limited number of experiments at this time several interesting wet oxidation phenomena have already been observed. The self-limiting oxidation effect could occur for wet oxidation at temperatures below \( \sim 750 °C \), which is very beneficial for fabricating controllable ultrafine SQWRs.

IV. CONCLUSIONS

We have successfully fabricated ultrafine SQWRs that have Si/SiO\textsubscript{2} interfaces as a physical boundary. It is accomplished by first growing a high quality Si/SiGe/Si heteroepitaxial film on a silicon substrate by VLP-CVD, and followed by lithography and reactive ion etching to form trench structures. Subsequent, selective chemical wet etching with a solution of HNO\textsubscript{3}:CH\textsubscript{3}COOH:diluted HF at 25 °C is applied to remove the Si\textsubscript{0.8}Ge\textsubscript{0.2} alloy layer and form silicon wires. Finally, two steps of wet and dry thermal oxidation are carried out to obtain ultrathin SQWRs having Si/SiO\textsubscript{2} interfaces. Excellent results are evidenced from SEM observation. Furthermore, the characteristic of wet oxidation of silicon wires was investigated, and it was also found that the self-limiting oxidation effect occurs for wet oxidation, which is important for controlling the lateral dimensions of SQWRs. The present work has clearly shown the success of combining SiGe/Si heteroepitaxy, selective chemical wet etching, and subsequent thermal oxidation as a very valuable method for fabricating ultrafine SQWRs.

ACKNOWLEDGMENTS

The authors would like to thank B. H. Mao and Z. H. Xie of Nanjing Electronic Device Institute for providing technical assistance. The work was supported by the Chinese National High-Technology R&D Program, the Chinese National Basic Science Research Program, and the Chinese National Natural Science Foundation.