# Simulation of a Ge–Si Hetero-Nanocrystal Memory

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***Abstract*—The Ge/Si hetero-nanocrystal as a floating gate has been discussed and improved. The charge stored in the quantum well formed by $SiO_2$–Ge–Si has to be thermally activated to the valence band of the Si nanocrystal before it can leak to the substrate which significantly reduces the leakage current from the charge storage node (nanocrystal) to the substrate. The simulation shows that the flash memory with Ge–Si (3 nm/3 nm) hetero-nanocrystal floating gates possesses a retention time of about ten years with a tunneling oxide of only 2 nm. Both writing and erasing speeds are fast in the Ge–Si hetero-nanocrystal memories, which is similar to that in the memory based on Si nanocrystals only.**

***Index Terms*—Erasing, hetero-nanocrystal memory, programming, retention.**

## I. Introduction

A SINGLE-ELECTRON memory is an ultimate device storing one-bit information by charging a single electron or hole. Due to the small size, and, therefore, small capacity (in the $10^{-15}$-F range), the Coulomb blockade effect [1] enables the multibit memory function. Owing to the low operation voltage, as well as the compatibility to the logical circuit, nanocrystal-based, especially Si-nanocrystal-based, MOS memories have been considered as one of the most promising applications in current very large scale integration (VLSI) [2]–[6]. In such a structure, Si nanocrystals are embedded in the $SiO_2$ matrix, shifting the threshold voltage if the nanocrystals are charged via tunneling injection through the oxide between the nanocrystals and the channel. As a nonvolatile memory device, the retention time at room temperature is one of the most important parameters. However, there is a tradeoff between the programming speed and the retention time. In order to have a long retention time, one needs to increase the tunneling oxide thickness. Nevertheless, a thicker tunneling oxide requires a higher operation voltage. A compromise would have to be achieved for a nanocrystal-based flash memory device. In order to have a higher programming speed, a longer retention time, and a lower operation voltage for scaling complementary metal–oxide–semiconductor (CMOS) platform, previously reported literatures considered the dielectrics multilayer instead of semiconductors [7]–[11]. For example, in [8] and [10], the authors used a "crested" multilayer tunneling barrier so that the sensitivity of the writing current on gate voltage can be improved. In [7] and [9], the nitride/oxide layered structure was implemented in the place of a single oxide tunneling barrier.

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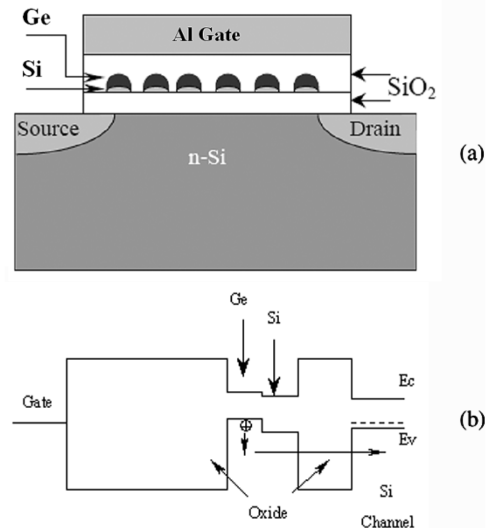


Fig. 1. (a) Schematic diagram of the p-channel memory device using Ge–Si as floating gates. (b) Energy-band structure of the memory.

This design results in a lower leakage current while keeping the same equivalent oxide thickness. A "quasi-superlattice" storage device was reported by Chang *et al.* [11], where the multilevel storage was realized by using an Si–$Si_3N_4$ superlattice. However, these designs need either complex fabrication processes [7], [9], [11] or very careful material selection, which needs more photo masks in addition to those used in the conventional Si CMOS process [8]–[10].

In contrast to using dielectric mutlilayer as barrier layers, a new structure is proposed by Yang *et al.* [12] using a semiconductor Ge–Si hetero-nanostructure as floating gate in which the Si also acts as a barrier layer for the holes during the data retention. Their calculation based on a Bardeen's transfer Hamiltonian method showed that this structure can significantly increase the retention time and keep the writing and erasing speeds changed insignificantly. In our previous work, we have compared the memory windows of a Ge–Si hetero-nanocrystal memory and an Si nanocrystal memory [13]. In this work, we present our physical model, which is extended to include the quantum confinement effect on the energy level of the hetero-nanocrystal, the thermal activation of the trapped hole in the nanocrystal, as well as the electron current during erasing. This model is believed to predict more reliable device operation results of a real device.

## II. Model and Theory

Fig. 1(a) shows the schematic diagram of a p-channel hetero-nanocrystal memory, and Fig. 1(b) shows the energy-band structure of the device using the Ge–Si hetero-nanocrystals as the floating gate [14]. We choose

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aluminum as the control gate electrode so that the flat-band voltage is around zero since both aluminum and our n-type silicon (doping concentration $3 \times 10^{17}$ cm$^{-3}$) have almost the same work function (4.28 eV for aluminum and 4.24 eV for Si here) [15]. During the retention, since it has cooled down to the ground state of the Ge dot, which is lower than the valence band edge ($E_v$) of the Si dot, the hole has to be thermally excited to the valence band edge of an Si nanocrystal first during the tunneling-back process from the Ge dot to the substrate, as shown in Fig. 1(b), which, in consequence, prolongs the retention time. In writing mode, the quantum confinement effect will also block the writing speed when the operation voltage is small since the $E_v$ of the nanocrystal is higher than that of the substrate. However, as the writing voltage increases to several voltages, this effect can be neglected. For the erasing mode, the current due to the tunneling of the electron from the substrate accumulation layer to the nanocrystal will be dominant. This is because of the fact that the band offset of the Ge–Si hetero-nanocrystal (0.47 eV) is higher than the difference (~0.1 eV) between the conduction band edges ($E_c$) for the nanocrystal and the accumulation layer where the electron has a higher density of states [two-dimensional (2-D)] than the hole in the nanocrystal [three-dimensional (3-D)]. Since the conduction band offset of Ge–Si is very small, the erasing process will be almost the same as that for a Si-nanocrystal-based memory. Thus both the writing and erasing processes are not influenced by using the Ge–Si hetero-nanocrystals as the floating gate in the place of Si nanocrystals.

Since the bias is applied between the control gate and the substrate, the lateral (dot-to-dot) charge exchange can be neglected. This is reasonable also due to the fact that the dot-to-dot spacing is generally one order of magnitude higher than the tunneling oxide thickness. Based on this assumption, a one-dimensional (1-D) model with some 3-D corrections is implemented for the calculation in this work, allowing only vertical charge transport via tunneling.

The time concept in a memory device can be defined as the inverse of the tunneling current density [15], [16]. Since the dot distribution is discrete and the dot size is small (~5 nm), the time $\tau$ is

$$\tau = \frac{q}{J \times L^2} \tag{1}$$

where $q$, $J$, and $L$ are the electron charge, tunneling current density, and the linear size of the nanocrystal, respectively. Only single-hole storage is considered here due to Coulomb blockade effect, which repulses the second hole to enter the dot once the nanocrystal is occupied by the first hole.

The writing and erasing tunneling current densities are calculated using the method proposed in [17] and [18], considering the quantization of carriers in the inversion layer or the accumulation layer when the device is biased

$$J = q \int_{E_{\text{shift}} \le E} T(E) f(E) \rho(E) F_{1/2}(E) dE \tag{2}$$

where $f(E)$ is the impact frequency, $\rho(E)$ is the 2-D density of states, $F_{1/2}(E)$ is the Fermi–Dirac distribution function, and $T(E)$ is the tunneling probability, respectively. $E_{\text{shift}}$ is the Si valence (for writing) or conduction band (for erasing) shift due to the quantum confinement effect from the small size of the nanocrystal. The impact frequency reads [18]

$$f(E) = 0.6 \times \frac{2q}{(3\pi\hbar m_{\text{Si},\perp})^{1/3}} \left(\frac{\varepsilon_{\text{ox}} F_{\text{ox}}}{\varepsilon_{\text{Si}}}\right)^{2/3} \tag{3}$$

where $\hbar, m_{\text{Si},\perp}, \varepsilon_{\text{ox}}, F_{\text{ox}}$, and $\varepsilon_{\text{Si}}$ are the reduced Planck's constant, the hole (or electron) effective mass perpendicular to the substrate, the dielectric constant of $SiO_2$, the surface electric field in the $SiO_2$ layer, and the Si dielectric constant, respectively. The density of states for a 2-D confined hole or electron gas is [18]

$$\rho(E) = \frac{m_{\text{Si},//}}{\pi\hbar^2} \tag{4}$$

where $m_{\text{Si},//}$ is the hole or electron effective mass in the confined plane of the accumulation or the inversion layer. The surface field of the oxide layer $F_{\text{ox}}$ is derived by solving the Poisson equation. The tunneling probability $T(E)$ was derived with the transfer matrix method [19], [20]. Briefly, an arbitrary barrier could be approximated with $N$ slices, within which slice the potential keeps a constant. The approximation can be sufficiently precise if $N$ is sufficiently large. The wave function with each potential sheet can be expressed as the sum of a forward and a backward wave. Using the boundary conditions for energy and momentum conservation yields the relation between the wave amplitudes in sheet $i$ and $i+1$, which finally leads to [20]

$$\begin{pmatrix} A_{N+1} \\ B_{N+1} \end{pmatrix} = T \begin{pmatrix} A_0 \\ B_0 \end{pmatrix} = \begin{pmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{pmatrix} \begin{pmatrix} A_0 \\ B_0 \end{pmatrix} \tag{5}$$

where $T$ is the transfer matrix and $A_i, B_i$ $(i = 1 \sim \text{N}+1)$, are the amplitudes of the forward and backward wave components in the $i$th slice in the barrier. Since $A_1 = 1$ and $B_n = 0$, which means a unit forward wave in the incident medium and there is no backward component at the exit side, one then obtains the tunneling coefficient $D(E_x)$ [19], [20] as

$$D(E_x) = \frac{k_{N+1}(E_x) \times m_0^*}{k_0(E_x) \times m_{N+1}^*} |A_{N+1}(E_x)|^2 \tag{6}$$

where the wave vector $k_i$ in the $i$th slice verifies

$$k_i = \frac{\sqrt{2m_i^*(E - V_i)}}{\hbar} \tag{7}$$

and $V_i$ is the potential in the $i$th potential sheet. The potential distributions for retention and writing/erasing processes are obtained by solving the Poisson equation with the finite-difference method by considering the contribution of the charge if it is already injected into the nanocrystal.

During retention at zero bias, the electron current from the substrate to the positively charged nanocrystal is very small due to the potential drop across the tunneling oxide. Therefore, the retention time is dominated by the hole current leakage from the nanocrystal to the substrate [21]. The retention time $\tau$ is derived with following method:

$$\tau = \frac{1}{\sum_{i=n}^{\infty} \exp\left(\frac{-(E_i - E_0)}{k_B T}\right) f(E_i) T(E_i)} \tag{8}$$

where $E_i, E_0$, and $K_B$ are the $i$th excited and ground states of the hetero-nanocrystal and Boltzmann's constant, respectively. The integer number $n$ is the quantum number from which the wave function of the hole covers both Ge and Si regions of the hetero-nanocrystal. Note that $E_n$ will automatically be greater than $E_v$ of the Si substrate, and, thus, the states with a quantum number higher than $n$ can tunnel to the Si substrate. The term $\exp(-(E_i - E_0)/k_BT)$ in (8) represents the detrapping coefficient since a hole confined in the Ge dot region should be first thermally activated to the $n$th excited state before it can tunnel to the substrate. This process is very similar to the process of an electron detrapping from the defect-related trapped state to the Si conduction band in an Si-nanocrystal-based memory device, as described by She *et al.* [21]. The eigen-energy levels and corresponding wave functions are calculated using an improved shooting method [23] with the effective mass approximation of charges in a cubic quantum box. The quantum box deviates from the real shape of nanocrystals; nevertheless, it provides a first-order accuracy.

For all of the calculations, the control oxide is fixed at 5 nm so that the tunneling through control oxide can be disregarded. All of the interfaces, including $SiO_2$–Si, Ge–Si, and Ge–$SiO_2$, are assumed to be abrupt to provide the first-order analysis. The cases that practical devices may have gradual interfaces due to intermixing and band-structure deformation due to strain built in Si and Ge are not considered. Although the intermixing of Ge–$SiO_2$ (tunneling oxide) has been reported to degrade the memory performance [22], it is not a serious issue in our case, since the oxide side of the Ge–$SiO_2$ interface here is control oxide. The effect of intermixing of Ge–Si on the ground state energy of a hole in the Ge region and the retention characteristics is an issue to be investigated. Due to the random orientation of nanocrystals, the effective masses of density of states were used for tunneling calculation. The values are 1.08 and 0.56 $m_0$ for electrons in Si and Ge, respectively, and 0.29 and 0.57 $m_0$ for holes in Si and Ge, respectively, where $m_0$ is the electron mass in free space.

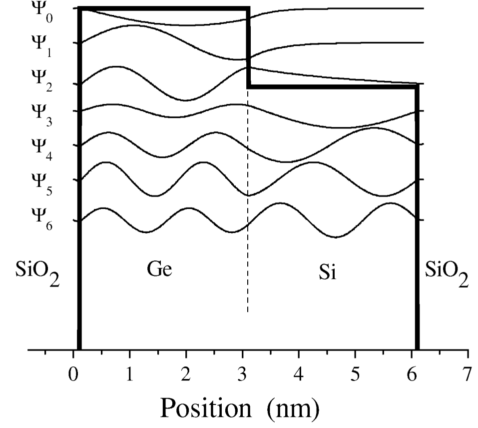


Fig. 2. Wave function within the $SiO_2$–Ge–Si–$SiO_2$ compound quantum well. From the third excited states, the wave functions become delocalized from the Ge region and covers the hole well region. The eigen-energy of the third state is now the valence band bottom.

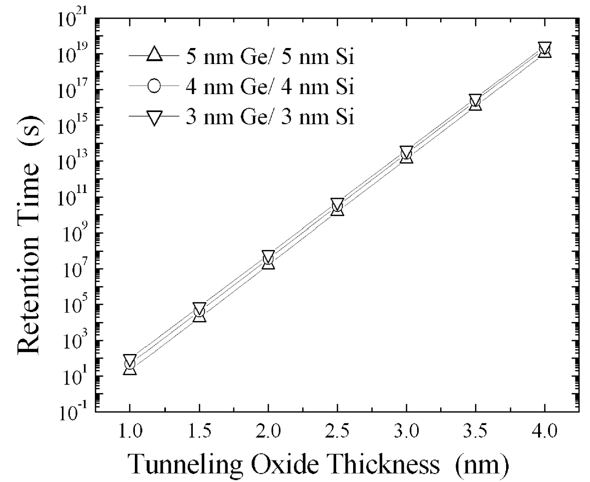


Fig. 3. Retention time of the Ge–Si hetero-nanocrystal flash memory as a function of the tunneling oxide thickness with different nanocrystal sizes. The difference due to the change of the nanocrystal size is insignificant. The retention time reaches ten years when a 2.0-nm tunneling oxide is used for a 3-nm Ge/3-nm Si hetero-nanocrystal p-channel flash memory.

## III. Results and Discussion

The normal components (to the Si–$SiO_2$ interface) of the hole wave function for the ground state and several exited states are given in Fig. 2 for the Ge–Si hetero-nanocrystal embedded in $SiO_2$, where both Ge dot and Si dot sizes are 3 nm. For simplicity, both Ge and Si nanocrystals are assumed to have cubic shapes. It is found the wave function is mainly localized in the Ge region when the quantum number $i$ is less than 3. For the third excited state, the wave function is delocalized from the Ge region and spreads to cover the Si region as well. The corresponding eigen-energy $E_3$ (the third excited state) is calculated to be 0.58 eV with the shooting method [23]. The ground state energy is 0.044 eV. The retention time thus is calculated as a function of the tunneling oxide thickness, as shown in Fig. 3, where the cases with 4-nm Ge/4-nm Si and 5-nm Ge/5-nm Si hetero-nanocrystals are also given. The retention time reaches $\sim 10^8$ s (ten years) when the tunneling oxide thickness is 2.0 nm. Due to the quantum confinement effect, the smaller dot leads to a shorter retention time, as shown in Fig. 3. The retention time for the device with 5-nm Ge/5-nm Si and a tunneling oxide of 2 nm is $6 \times 10^7$ s, which is slightly smaller than the value ($1.1 \times 10^8$ s) obtained in [12] where the quantum confinement was not considered. However, it is also found from Fig. 3 that the retention time is only slightly improved by employing a larger nanocrystal. This dot-size immunity of the retention time benefits the device performance uniformity since the real fabrication of the nanocrystal will more or less introduce a certain dot-size distribution, which, in consequence, leads to a device performance dispersion particularly when the device scales down to include only several nanocrystals.

As a comparison, the corresponding retention times for the memory device using Si nanocrystals only are illustrated in Fig. 4. Due to the quantum confinement mechanism, $E_v$ (ground state) of the Si nanocrystal is higher than that of the Si substrate. For a 6-nm cubic Si nanocrystal embedded in $SiO_2$, the ground state of the hole is calculated to be 0.056 eV higher than the $E_v$ of the Si substrate. Therefore, a resultant tunneling oxide thickness of $\sim$3.4 nm is required for a ten-year

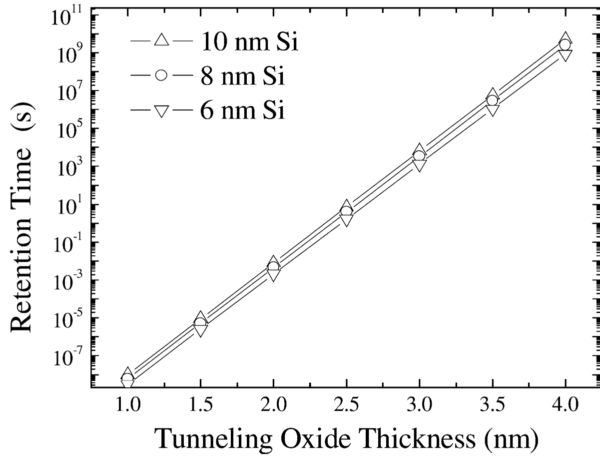


Fig. 4. Retention time of an Si nanocrystal flash memory as a function of the tunneling oxide thickness with difference nanocrystal sizes. The difference due to the change of the nanocrystal size is also insignificant. The retention time in this case is much less than the case of the hetero-nanocrystal.

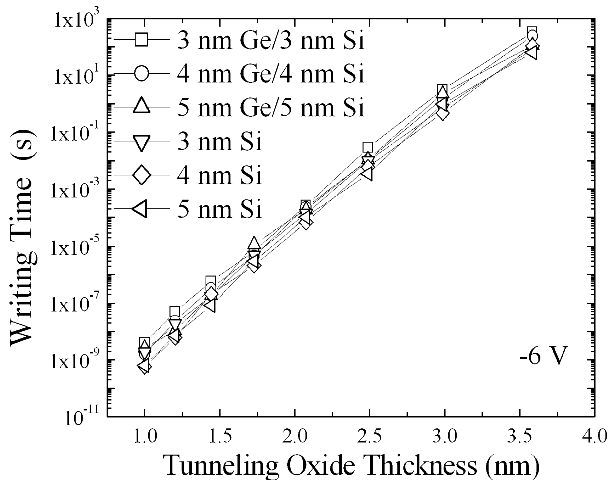


Fig. 5. Writing time as a function of the tunneling oxide thickness for both the Si nanocrystal and the Ge–Si hetero-nanocrystal memories. The dependences of the writing time on both crystal size and the Ge presence are all very slight.

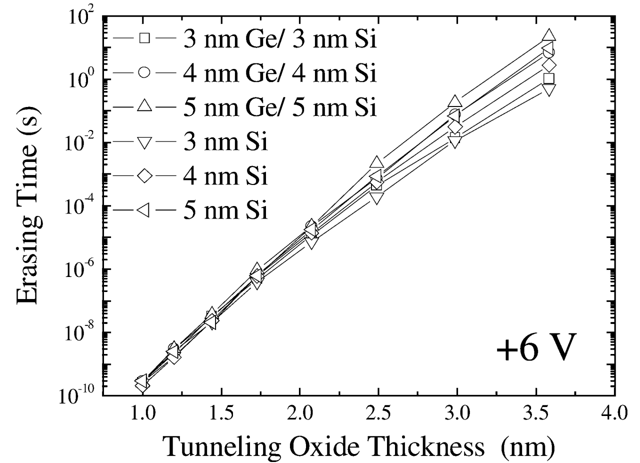


Fig. 6. Erasing time as a function of the tunneling oxide thickness for both the Si nanocrystal and the Ge–Si hetero-nanocrystal memories. The crystal size and the presence of a Ge dot on an Si dot does not affect the erasing process.

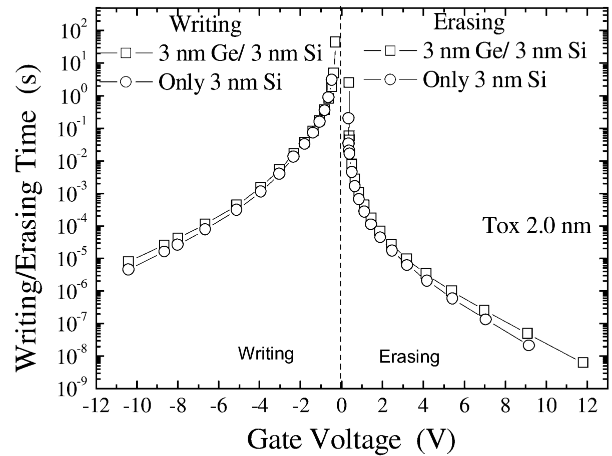


Fig. 7. Dependence of the programming speeds on the operation voltage. Due to a higher hole barrier, writing a hole to the dot is more difficult than erasing it.

retention if the Si nanocrystal only is present, seen in Fig. 4, which means a much higher programming voltage for keeping a decent programming speed.

Fig. 5 shows the writing time as a function of the tunneling oxide thickness for both Ge–Si hetero-nanocrystal and Si nanocrystal memories with a writing voltage of $-6$ V. Again, only very small differences can be found for different nanocrystal sizes. The difference between the memory devices with and without the hetero-nanocrystals is also not remarkable, which means that the influence of the hetero-structure on the writing speed can be neglected. However, due to the higher barrier (5.1 eV) for a hole than that for an electron (3.1 eV), the p-channel memory device proposed here has a relatively lower writing speed ($\sim 5 \times 10^{-5}$ s at $-6$ V) than an n-channel device ($\sim 1 \times 10^{-6}$ s at 6 V, in [21]).

The erasing time is shown in Fig. 6 with an operation voltage of 6 V as a function of the tunneling oxide thickness for both the cases of Ge–Si hetero-nanocrystals and Si nanocrystals, with different nanocrystal sizes. The erasing time difference tends to be greater as the tunneling oxide thickness increases. An erasing time around 1 $\mu$s can be achieved with a tunneling oxide thickness of around 2.0 nm.

The voltage dependences of the writing and erasing processes are illustrated in Fig. 7, where Ge and Si are both 3 nm thick and the tunneling oxide is kept as 2.0 nm. It is found again, for both the writing and erasing processes, that the Ge on the Si nanocrystal does not influence the speed. As the writing voltage increases to $-10$ V, the writing time can be improved to be several microseconds while the erasing time can be 0.03 $\mu$s as the erasing voltage equals 10 V.

## IV. Conclusion

By introducing the Ge–Si hetero-nanocrystals in a p-channel flash memory device, an extra quantum well for the holes is established [12]. This model is improved to include the quantum confinement effect and both electron and hole currents during device operation. The dependence of the retention, writing and erasing times on the hetero-structure, the tunneling oxide thickness, and the nanocrystal size were investigated, respectively. Calculations show that the existence of this type of quantum

well will benefit the retention time prominently while not interfering with the writing and erasing speeds.

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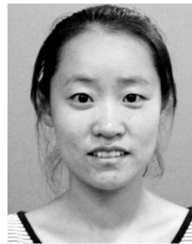

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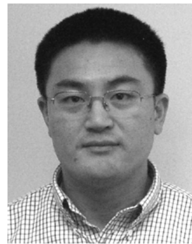

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