High-density NiSi nanocrystals embedded in Al₂O₃/SiO₂ double-barrier for robust retention of nonvolatile memory

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Abstract

NiSi nanocrystals of high density and good uniformity were synthesized by vapor–solid–solid growth in a gas source molecular beam epitaxy system using Si₂H₆ as Si precursor and Ni as catalyst. A metal–oxide–semiconductor memory device with NiSi nanocrystal–Al₂O₃/SiO₂ double-barrier structure was fabricated. Large memory window and excellent retention at both room temperature and high temperature of 85°C were demonstrated.

1. Introduction

Nonvolatile memories with discrete charge storage nodes have been investigated extensively during the past decade. Since it was pioneered by Tiwari in 1995[1], Si nanocrystal (NC) floating gate memory has been nominated as a promising replacement of conventional flash memory thanks to its immunity to defect-related charge leakage and potential to exceed flash scaling limit. Both academia and industry have also invested tremendous efforts into research of other NC memories, exploring new materials and novel gate structures for future flash memory[2–9]. Metal silicide N Cs, with high density of states and robust thermal stability, have attracted much attention since they were proposed as good candidates to improve NC memory performance[10] and much work has been done to explore this material for nonvolatile memory application[11–18]. As an alternative way of improving memory performance, NC core–shell structure with additional barrier layer as floating gate has been developed and adopted by researchers. For example, metal and semiconductor NC core with oxide shell synthesized by various methods such as laser irradiation induced native oxidation[19], micelle dipping[20], chemical vapor deposition and annealing[21] and pulsed laser deposition[22] were reported.

In this paper, we report a metal–oxide–semiconductor capacitor memory device with an engineered floating gate similar to core–shell structures. The floating-gate structure consists of a layer of high-density vapor–solid–solid (VSS) induced NiSi NCs by gas source molecular beam epitaxy (GSMBE) embedded in-between two Al₂O₃ thin barriers deposited by atomic layer deposition (ALD). Fig. 1a shows a schematic diagram of the device structure. The Al₂O₃/NiSi NC/Al₂O₃ floating gate is sandwiched by a control oxide layer and a tunnel oxide layer. Fig. 1b shows the flat energy band diagram of the memory device. The Fermi-level of NiSi NC with a work function of 4.7 eV[23] is aligned within the mid-gap of bulk Si. The conduction band offset between NiSi and Al₂O₃ (electron affinity 1.35 eV, Ref.[24]) is as high as 3.35 eV. The benefit of using additional Al₂O₃ barrier layers is two folds. First, it is to minimize diffusion of Ni metal atoms into SiO₂ tunneling layer during high temperature process to reduce the charge leakage paths for prolonged retention. Second, it is to maintain programming efficiency and improve retention performance. Energy band diagrams of programming and retention states are illustrated in Fig. 1c. During programming, gate bias is applied so that electrons can be pulled into NCs by Fowler–Nordheim tunneling. Because of the high-K property of Al₂O₃, electric field concentration effect[25] makes most of the voltage drop on SiO₂ layer. In addition, since the barrier height of Al₂O₃ layer is lower than that of SiO₂, electrons do not actually have to go through the barrier of Al₂O₃ but only the thin SiO₂ tunnel barrier to reach the NC. Hence, it is believed that this structure has...
the ability to maintain the efficiency of programming operation compared to the structure without Al2O3. On the other hand, in retention state, electrons are kept in the deep quantum well formed by Al2O3/NiSi NC/Al2O3 structure. In this case, electrons see a barrier of both Al2O3 and SiO2 and the total barrier thickness is increased. Therefore, robust retention characteristics are expected for this Al2O3/NiSi NCs/Al2O3 floating-gate memory device combining metallic silicide NCs with double-barrier structure.

2. Device fabrication

Device fabrication starts with a pre-cleaned p-type Si (100) substrate. A thin thermal oxide of 3 nm was grown on the substrate at 850 °C. This was followed by 2.5 nm Al2O3 deposition using ALD. A very thin layer of Ni was coated on the sample by room temperature electron-beam evaporation as catalyst and the sample was immediately transferred into a custom-built GSMBE system for subsequent silicide NC synthesis. Disilane (Si2H6) was used as the Si precursor to perform VSS growth at 600 °C, which is a temperature much lower than the eutectic temperature between Ni and Si of 964 °C [26]. Growth conditions (i.e. growth time, gas source flux) were calibrated to achieve reliable high-density ultra-uniform NCs growth over the whole sample surface. After NiSi NCs formation, another thin Al2O3 layer of 4.5 nm was deposited.

![Schematic of device structure](image)

Fig. 1. (a) Schematic of device structure; (b) flat energy band diagram of NiSi NC-Al2O3 floating-gate memory; and (c) energy band diagram at programming and retention states.
on top by ALD to form the Al₂O₃/NiSi NC/Al₂O₃ structure. Finally, 25 nm SiO₂ was deposited as control oxide in a low pressure chemical vapor deposition (LPCVD) system and Al was evaporated onto the front and back side of the sample as contacts for the memory capacitors. Control device without NC embedded in Al₂O₃ and NC device without Al₂O₃ were fabricated simultaneously for comparison.

3. Results and discussion

Fig. 2a shows a scanning electron microscopy (SEM) image of the as-grown NCs on Al₂O₃ surface. The average size of uniformly distributed NCs over the whole sample surface is about 4.5 nm and the density is around $1.5 \times 10^{12}$ cm$^{-2}$. X-ray photoelectron spectroscopy (XPS) was utilized to determine the chemical nature of the NCs. Fig. 2b shows the XPS result of Ni 2p3/2 for the sample before top Al₂O₃ coverage. The binding energy peak found at 853.9 eV indicates that the nature of NC is NiSi[27]. Fig. 2c and d shows the cross-sectional transmission electron microscopy (TEM) images of the NC core–shell memory device and the control device without NC, respectively, where the interfaces are edge-on and the thickness of each layer in the devices could be measured directly from the images. The TEM images indicate that the interfaces are flat, and layer thicknesses are consistent with the designed ones, as mentioned above.

Fig. 3a and b shows high-frequency (1 MHz) capacitance–voltage (C–V) sweep characteristics of NiSi NC–Al₂O₃ floating-gate memory and its non-NC control device, respectively. With gate voltage increasing from 24 V/-30 V to 34 V/-40 V, the memory window increases from 1.4 V to 15 V, suggesting that the memory effect is due to the NC storage rather than defect/interface state charging. The large memory window also suggests high charge storage capability of the NiSi NCs. In comparison, with the same gate voltage sweeping range, almost no memory window was observed in the control device without NCs, which confirms that memory window shown by the core–shell memory device is attributed to charge storage in the NCs. The high voltage required for C–V sweeping here is due to the thick control oxide layer deposited by LPCVD. With optimized device geometry, it is expected that lower gate voltage operation and shorter programming/erasing time can be achieved.

Fig. 4a shows flat-band voltage shift ($\Delta V_{FB}$) as a function of programming/erasing time under different gate voltages. Programming was conducted by biasing the gate with a positive voltage while a negative voltage was applied for erasing. Clear time dependence of $\Delta V_{FB}$ was observed in both programming and erasing case for gate voltage ±21 V to ±24 V. The lower speed of erasing than that of programming is due to the deep quantum well formed in the Al₂O₃/NiSi NC/Al₂O₃ structure, which makes electron see higher and thicker barrier in erasing. It should also be noticed from the curves that higher voltage results in larger $\Delta V_{FB}$, suggesting a voltage-dependent programming/erasing behavior of the memory device. Fig. 4b shows the $\Delta V_{FB}$ and number of electrons per NC as a function of writing voltage. The charge stored per unit area in a device is calculated from: $Q = (\varepsilon_{SiO_2}/\varepsilon_{SiO_2})\Delta V_{FB}$, where $\varepsilon_{SiO_2}$ is the dielectric constant of SiO₂, $d_{SiO_2}$ is the equivalent control oxide thickness of the MOS device, which is 27 nm in this work, and $\Delta V_{FB}$ is the $V_{FB}$ shift between fresh state and programmed state. The charge number per NC is calculated from: $\#\text{ of electrons/dot} = Q/d$, where $D$ is the NC density, which is $1.5 \times 10^{12}$ cm$^{-2}$ here and
based on which a nonvolatile memory with Al₂O₃/ NiSi NC/ Al₂O₃ structure as floating gate was fabricated and characterized. The memory device exhibits large memory window, robust retention at both room temperature and high temperature of 85 °C, and good endurance. Further device geometry optimization of using thinner control oxide and varied Al₂O₃ thickness may be carried out to achieve low voltage operation as well as good transient performance. Memories with this structure can be a promising candidate for future flash memory application.

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References


Fig. 6. Endurance characteristics of NiSi NC-Al₂O₃ floating-gate memory up to 10⁸ cycles.

4. Conclusions

NiSi NCs of high density and good uniformity were synthesized by VSS growth in a GSMBE system using Si₂H₆ as Si precursor, which is the electron charge. More than 5 electrons can be injected into each NC on average before saturation, indicating good charge holding capability of NiSi NCs similar to other metallic silicide NCs [16].