Memory characteristics of ordered Co/Al_2O_3 core-shell nanocrystal arrays assembled by diblock copolymer process

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(Received 27 October 2010; accepted 15 April 2011; published online 11 May 2011)

An ordered Co/Al_2O_3 core-shell nanocrystal (NC) nonvolatile memory device was fabricated. Self-assembled diblock copolymer process aligned the NCs with uniform size. Co/Al_2O_3 core-shell NCs were formed using atomic layer deposition of Al_2O_3 before and after the ordered Co NC formation. Compared to Co NC memory, Co/Al_2O_3 core-shell NC memory shows improved retention performance without sacrificing writing and erasing speeds. © *2011 American Institute of Physics*. [doi:10.1063/1.3589993]

Nonvolatile memory devices with floating-gate structure are being widely used in MP3 players, digital cameras, and memory cards nowadays.[1] The most prominent problem of poly-Si floating gate memory is the limited potential in continuous scaling of the device structure.[2] Due to excellent memory performance and high scalability, nanocrystal (NC) floating gate memory devices have attracted considerable attention.[3] Different types of NCs such as double Si dots,[4] Ge NCs,[5] metal NCs,[6–8] silicide NCs,[9–12] and dielectric NCs (Ref. 13) have been proposed to achieve memory devices with longer retention performance. Among these NCs, metallic NCs have larger work function than the electron affinity of Si NCs, and are advantageous to reduce the leakage current through the tunneling barrier due to increased barrier height.[14] These NC memories also achieved high programming/erasing (P/E) speeds based on the high density of states in NC storage.[15,16] Nevertheless, all NCs are randomly distributed, limiting the device performance and overall scalability. The synthesis of uniform, well ordered NC arrays is one of the key limitations for device fabrication, garnering much of the research focus at the moment.[17,18] Additionally, as the memory technology scales down further, thinner SiO_2 tunnel layer is required for lower power operations. However, thinner oxide increases leakage, leading to compromised retention. It is well known that leakage current of high-k materials is smaller than that of SiO_2 for the same equivalent oxide thickness (EOT). To improve the retention performance of memory devices, recent studies have tried to use high-k dielectrics such as Al_2O_3 and HfO_2, instead of SiO_2 layers, for the tunnel and control oxide layers to reduce the leakage.[19]

In this letter, we developed Co NC ordered arrays with uniform size and distribution using a diblock copolymer synthesis process. In addition, thin Al_2O_3 high-k layers were deposited by atomic layer deposition (ALD) as shell of the NCs. The purpose is twofold; the ability of minimizing segregation of Co metal atoms to tunnel oxide during high-temperature device process and the increase in EOT. The benefit is enhanced retention performance. Uniformly distributed Co/Al_2O_3 core-shell NCs are embedded in metal-oxide-semiconductor (MOS) memory system. The Co/Al_2O_3 core-shell NC memory achieved a higher retention performance as compared to Co NC memory reference sample.

A self-assembly diblock copolymer process was used to deposit highly ordered Co NC arrays. First, a 3.0-nm-thick thermal oxide was grown in dry oxygen at 850 °C as the tunnel oxide. A thin Al_2O_3 layer approximately 1 nm thick was then deposited on the SiO_2 layer by ALD at 250 °C, using Cambridge Savannah 100&200. Self-assembly of Co NCs was achieved by mixing PS-b-P4VP, toluene, and $CoCl_2 \cdot 6H_2O$ for 48 h, followed by spin-coating onto the sample surface. The polymer was subsequently removed by exposure to oxygen plasma for 3 min. The obtained Co NCs were reduced from CoO by performing a forming gas annealing at 400 °C for 30 min. A layer of Al_2O_3, approximately 1 nm, was deposited over the Co NC array to encapsulate the particles and form the desired core-shell structure. A control oxide layer of about 15 nm was then deposited by low pressure chemical vapor deposition (LPCVD) and then electrode was patterned to form MOS structure memory capacitor. Additionally, a sample with only Co NCs and another sample with pure Al_2O_3 were prepared as reference samples to compare their device performances.[20]

Figures 1(a) and 1(b) show scanning electron micro-

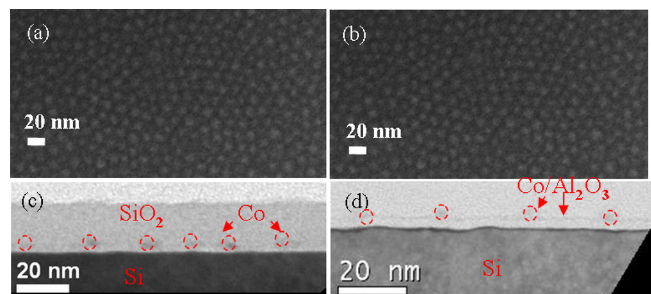

FIG. 1. (Color online) (a) SEM image of ordered Co NCs on SiO_2. Diblock copolymer remains on the surface, (b) SEM image of ordered Co NCs on Al_2O_3. Diblock copolymer remains on the surface, (c) TEM image of Co NC memory, (d) TEM image of Co/Al_2O_3 core-shell NC memory.

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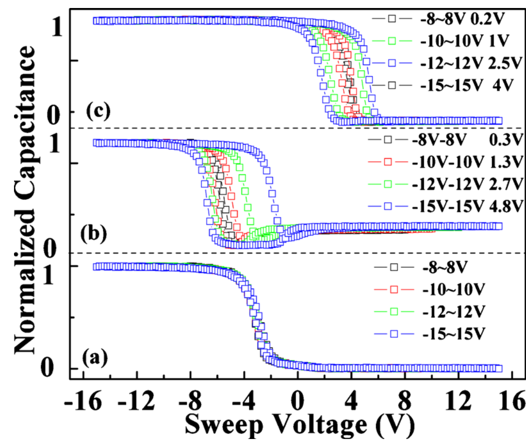

FIG. 2. (Color online) Normalized C-V sweep result for capacitor memories with (a) Al_2O_3 shell only, (b) Co NCs, and (c) Co/Al_2O_3 core-shell NCs. The size of top contact is 100×100 μm^2.

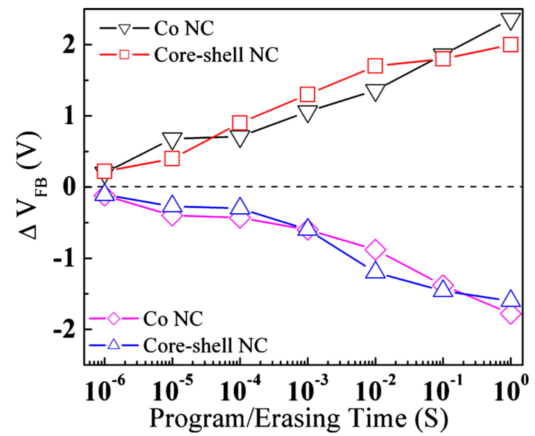

FIG. 3. (Color online) P/E transient characteristics for capacitor memories with Co/Al_2O_3 core-shell NCs and Co NCs without shell.

scope (SEM) images of Co NCs on SiO_2 and Co NCs on Al_2O_3 aligned with the diblock copolymer process, respectively. The NC arrays are well ordered with uniform size and spacing between particles, resulting in a density of $\sim5\times10^{11}$ NCs/cm^2 in both cases. Figures 1(c) and 1(d) show the cross-sectional transmission electron microscope (TEM) images of Co NC memory and Co/Al_2O_3 core-shell NC memories after device fabrication, respectively. Based on these measurements, the average diameter of the spherical NCs is determined to be ~6 nm with an average distance spacing of ~14 nm. The thickness of the tunnel oxide is ~3 nm and the control oxide is ~15 nm. As shown in Fig. 1(d), thin Al_2O_3 shell layer is clearly shown between the Co dots, indicating the existence of Al_2O_3 layer. Further energy dispersive x-ray spectroscopy analysis proved the existence of core-shell structure.[20]

The MOS capacitor memories were characterized using an Agilent LCR meter at room temperature. A typical high-frequency (1 MHz) capacitance-voltage (C-V) sweep results with a scanning range between ±8 V and ±15 V for the devices with Al_2O_3 shell only, Co NCs and Co/Al_2O_3 core-shell NCs are shown in Figs. 2(a)–2(c), respectively. The sweep started from the inversion to the accumulation, and finally back to the inversion region at a rate of 0.5 V/s.

In Fig. 2(a), as voltage is swept from (−8)−(8) V, (−10)−(10) V, (−12)−(12) V, and (−15)−(15) V, a tiny memory window (~0.2 V at ±15 V sweep) is shown, which may be caused by defects in the Al_2O_3 layer. As the NCs are added to the device structure, an obvious hysteresis is observed as the gate voltage increases [Fig. 2(b)]. Starting at ±8 V, the memory window is estimated to be ~0.3 V. Increasing the sweep voltage range to 10 V, 12 V, and 15 V resulted in a memory window increase of 1.2 V, 2.7 V, and 4.8 V, respectively. Figure 2(c) shows obvious hysteresis curves at different sweep voltages. A small memory window of ~0.2 V is obtained as the voltage is swept at ±8 V. As the sweep voltage range increases to 10 V, 12 V, and 15 V, the memory window increases to 1 V, 2.5 V, and 4 V, respectively. Wider voltage sweep range leads to the fact that more electrons are programmed to the NCs and erased from the NCs, therefore larger memory window is achieved. It should be noted that overall shift of hysteresis curves of Fig. 2(c) to the right compared with those in Fig. 2(a) and Fig. 2(b) may be due to the additional trapping of charges in $SiO_2/Al_2O_3/Co$ interfaces.

Figure 3 shows the flat band voltage shift, Fig. 2(c), changes with P/E time for Co and Co/Al_2O_3 core-shell NC memory, respectively, when using a P/E voltage of ±15 V. As programming time increases, more electrons are injected into the NCs until a saturation is achieved and, no more electrons are able to enter the NCs. The same situation is observed as the device is erased. As the erasing time increases, more electrons are extracted from the NC core-shell structures. Although core-shell NC memory has additional Al_2O_3 shell layer, electric field concentration effect[21] caused by the high-k properties makes most of the voltage drop on SiO_2 layer. This makes Co NC memory and Co/Al_2O_3 core-shell NC memory appear to have similar P/E speeds.

Figure 4 shows retention characteristics of the two capacitor memories with Co and Co/Al_2O_3 core-shell NCs at programmed and erased states, respectively. The P/E conditions are 15 V and −15 V for 1 s, respectively. After programming, transient capacitance at the same read voltage is recorded intermittently. The Co/Al_2O_3 core-shell NC capacitor memory leads to a slower charge loss ratio. After $\sim10^5$ s, ~70% charge is left in the Co/Al_2O_3 core-shell NC memory capacitor and ~50% charge is left in the Co NC capacitor memory, which is reasonable for a tunnel oxide of 3 nm. The electrons are confined in the Co NCs and high-k Al_2O_3 shell acts as an additional barrier to the electrons com-

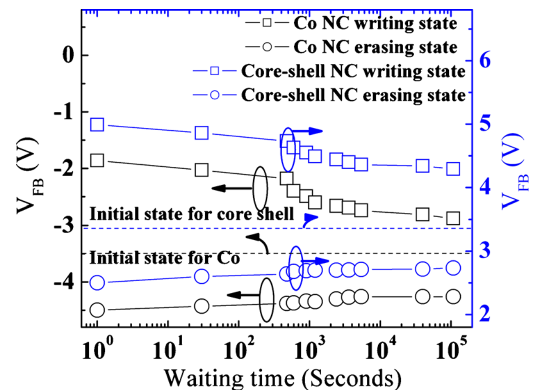

FIG. 4. (Color online) Retention characteristics for capacitor memories with Co/Al_2O_3 core-shell NCs and Co NCs without shell.

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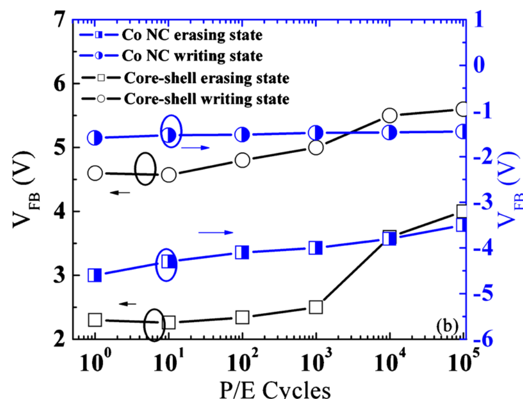

FIG. 5. (Color online) Endurance characteristics for capacitor memories with Co/Al_2O_3 core-shell NCs and Co NCs without shell.

pared to the Co NC memory, which contributes to the slower charge loss ratio and longer retention time.

Figure 5 shows the endurance characteristics of the two capacitors with Co and Co/Al_2O_3 core-shell NCs, respectively. The P/E conditions are ±16 V for 200 ms. The memory windows of the two devices stay open up to 10^5 times of operation, although the magnitude shrinks about 23%. The up-shift of the flat band voltage with times of operation is due to the accumulated trapped charges in the Al_2O_3 layer.

In summary, a core-shell NC MOS memory was demonstrated. Uniform NC size and spacing are obtained by a diblock copolymer fabrication process. The uniform NC distribution throughout the sample is critical for device scalability, reliability, and manufacturability. High-k Al_2O_3 layer is used as shell in the core-shell structure, which improves the retention performance. Reliable diblock copolymer process to make metal/high-k core-shell NC memory may open up opportunities for memory applications.

The authors acknowledge the financial and program support of the Microelectronics Advanced Research Corporation (MARCO) and its Focus Center on Function Engineered NanoArchitectonics (FENA), the DARPA/Defense Microelectronics Activity (DMEA) under Agreement No. H94003-10-2-1003 and the National Science Foundation (Grant No. DMR-0807232). The TEM work was performed on Philips CM-20 TEM in Materials Characterization Center at UCI.

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